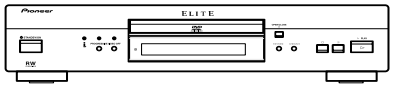
Pioneer sound.vision.soul

Service Manual



DV-47Ai

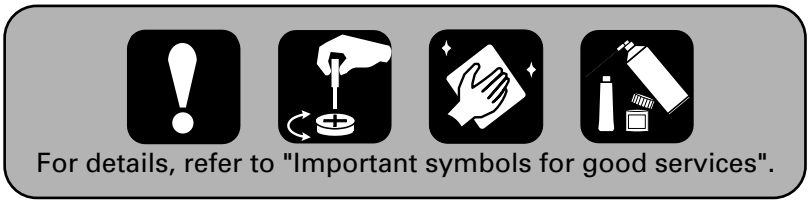
ORDER NO.
RRV2650

DVD PLAYER

DV-47Ai

THIS MANUAL IS APPLICABLE TO THE FOLLOWING MODEL(S) AND TYPE(S).

Model	Type	Power Requirement	Regional restriction codes (Region No.)	Remarks
DV-47Ai	KUXJ/CA	AC120V	1	



PIONEER CORPORATION 4-1, Meguro 1-chome, Meguro-ku, Tokyo 153-8654, Japan
PIONEER ELECTRONICS (USA) INC. P.O. Box 1760, Long Beach, CA 90801-1760, U.S.A.
PIONEER EUROPE NV Haven 1087, Keetberglaan 1, 9120 Melsele, Belgium
PIONEER ELECTRONICS ASIACENTRE PTE. LTD. 253 Alexandra Road, #04-01, Singapore 159936

T-ZZE AUG. 2002 printed in Japan

SAFETY INFORMATION

This service manual is intended for qualified service technicians; it is not meant for the casual do-it-yourselfer. Qualified technicians have the necessary test equipment and tools, and have been trained to properly and safely repair complex products such as those covered by this manual.
Improperly performed repairs can adversely affect the safety and reliability of the product and may void the warranty. If you are not qualified to perform the repair of this product properly and safely, you should not risk trying to do so and refer the repair to a qualified service technician.

WARNING
This product contains lead in solder and certain electrical parts contain chemicals which are known to the state of California to cause cancer, birth defects or other reproductive harm.

Health & Safety Code Section 25249.6 – Proposition 65

NOTICE
(FOR CANADIAN MODEL ONLY)
Fuse symbols (fast operating fuse) and/or (slow operating fuse) on PCB indicate that replacement parts must be of identical designation.

REMARQUE
(POUR MODÈLE CANADIEN SEULEMENT)
Les symboles de fusible (fusible de type rapide) et/ou (fusible de type lent) sur CCI indiquent que les pièces de remplacement doivent avoir la même désignation.

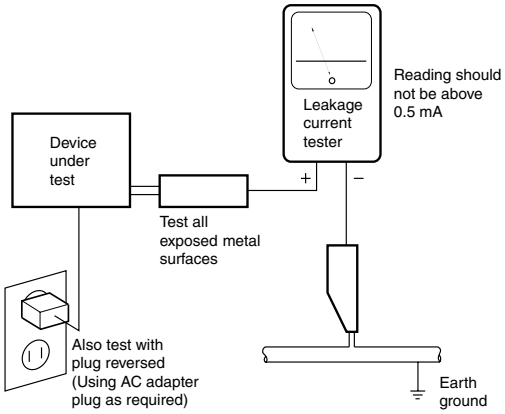
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60 Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5 mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.
The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

[Important symbols for good services]
In this manual, the symbols shown-below indicate that adjustments, settings or cleaning should be made securely.
When you find the procedures bearing any of the symbols, be sure to fulfill them:

1. Product safety

You should conform to the regulations governing the product (safety, radio and noise, and other regulations), and should keep the safety during servicing by following the safety instructions described in this manual.

2. Adjustments

To keep the original performances of the product, optimum adjustments or specification confirmation is indispensable. In accordance with the procedures or instructions described in this manual, adjustments should be performed.

3. Cleaning

For optical pickups, tape-deck heads, lenses and mirrors used in projection monitors, and other parts requiring cleaning, proper cleaning should be performed to restore their performances.

4. Shipping mode and shipping screws

To protect the product from damages or failures that may be caused during transit, the shipping mode should be set or the shipping screws should be installed before shipping out in accordance with this manual, if necessary.

5. Lubricants, glues, and replacement parts

Appropriately applying grease or glue can maintain the product performances. But improper lubrication or applying glue may lead to failures or troubles in the product. By following the instructions in this manual, be sure to apply the prescribed grease or glue to proper portions by the appropriate amount.For replacement parts or tools, the prescribed ones should be used.

CONTENTS

SAFETY INFORMATION 2
1. SPECIFICATIONS 5
2. EXPLODED VIEWS AND PARTS LIST 6
2.1 PACKING 6
2.2 EXTERIOR SECTION 8
2.3 FRONT PANEL SECTION 10
2.4 LOADING MECHA ASSY 12
2.5 TRAVERSE MECHANISM ASSY-S 14
3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM 16
3.1 BLOCK DIAGRAM 16
3.2 LOAB ASSY and OVERALL WIRING DIAGRAM 20
3.3 DVDM ASSY 1/4 [FTS BLOCK] 22
3.4 DVDM ASSY 2/4 [FR BLOCK] 24
3.5 DVDM ASSY 3/4 [EBY/AV1 BLOCK] 26
3.6 DVDM ASSY 4/4 [VENC BLOCK] 28
3.7 JACB ASSY 1/2 [AUDIO BLOCK] 30
3.8 JACB ASSY 2/2 [VIDEO BLOCK] 32
3.9 SACDB ASSY 34
3.10 FLKY and KEYB ASSYS 36
3.11 ILKB ASSY 38
3.12 POWER SUPPLY UNIT 40
3.13 WAVEFORMS [DVDM ASSY] 41
3.14 WAVEFORMS [JACB ASSY] 42
4. PCB CONNECTION DIAGRAM 43
4.1 LOAB ASSY 43
4.2 DVDM ASSY 44
4.3 JACB ASSY 46
4.4 SACDB ASSY 50
4.5 ILKB ASSY 51
4.6 FLKY and KEYB ASSYS 52
4.7 POWER SUPPLY UNIT 54
5. PCB PARTS LIST 55
6. ADJUSTMENT 59
6.1 ADJUSTMENT ITEMS AND LOCATION 59
6.2 JIGS AND MEASURING INSTRUMENTS 59
6.3 NECESSARY ADJUSTMENT POINTS 60
6.4 TEST MODE 61
6.5 MECHANISM ADJUSTMENT 62
7. GENERAL INFORMATION 65
7.1 DIAGNOSIS 65
7.1.1 ID NUMBER AND ID DATA SETTTING 65
7.1.2 SELF-DIAGNOSIS FUNCTION OF PICKUP DEFECTIVE 67
7.1.3 TEST MODE SCREEN DISPLAY 68
7.1.4 SELF-DIAGNOSIS FUNCTION 70
7.1.5 FUNCTION SPECIFICATION OF THE SERVICE MODE 71
7.1.6 ERROR DISPLAY 72
7.1.7 TEST POINTS LOCATION & WAVEFORMS 75
7.1.8 TROUBLE SHOOTING 77
7.1.9 DISASSEMBLY 79
7.2 IC 88
7.3 DISC / CONTENT FORMAT PLAYBACK COMPATIBILITY 143
7.4 CLEANING 144
8. PANEL FACILITIES 145

1. SPECIFICATIONS

General

System ..... DVD Player
Power requirements
DV-47Ai ..... AC 120 V, 60 Hz

Power consumption
DV-47Ai ..... 14 W

Power consumption (standby) ..... 0.4 W
Weight
DV-47Ai ..... 5.1 kg (11lb 3oz)

Dimensions
DV-47Ai ..... 420 (W) x 103 (H) x 278 (D) mm
(16 3/4 (W) x 4 1/8 (H) x 11 1/8 (D) in.)

Operating temperature ..... +5°C to +35°C
(+36°F to +96°F)
Operating humidity ..... 5% to 85%
(no condensation)

Component Video output (Y, P_B, P_R)

Output level ..... Y: 1.0 Vp-p (75 Ω)
P_B, P_R: 0.7 Vp-p (75 Ω)
Jacks ..... RCA jacks

S-Video output

Y (luminance) - Output level ..... 1 Vp-p (75 Ω)
C (color) - Output level ..... 286 mVp-p (75 Ω)
Jack ..... S-Video jack

Video output

Output level ..... 1 Vp-p (75 Ω)
Jack ..... RCA jack

Audio output (1 stereo pair)

Output level ..... During audio output
200 mVrms (1 kHz, –20 dB)
Number of channels 2
Jacks ..... RCA jack

Audio output (multi-channel / L, R, C, SW, LS, RS)

Output level ..... During audio output
200 mVrms (1 kHz, –20 dB)
Number of channels 6
Jacks ..... RCA jack

Audio characteristics

Frequency response
..... 4 Hz to 44 kHz(DVD fs: 96 kHz)
..... 4 Hz to 88 kHz (DVD-Audio fs: 192 kHz)
S/N ratio ..... 118 dB
Dynamic range ..... 108 dB
Total harmonic distortion ..... 0.0009 %
Wow and flutter ..... Limit of measurement
(0.001% W. PEAK) or lower

Digital output

Optical digital output ..... Optical digital jack
Coaxial digital output ..... RCA jack

Other terminals

Control in ..... Minijack (3.5 ø)
Control out ..... Minijack (3.5 ø)

Accessories

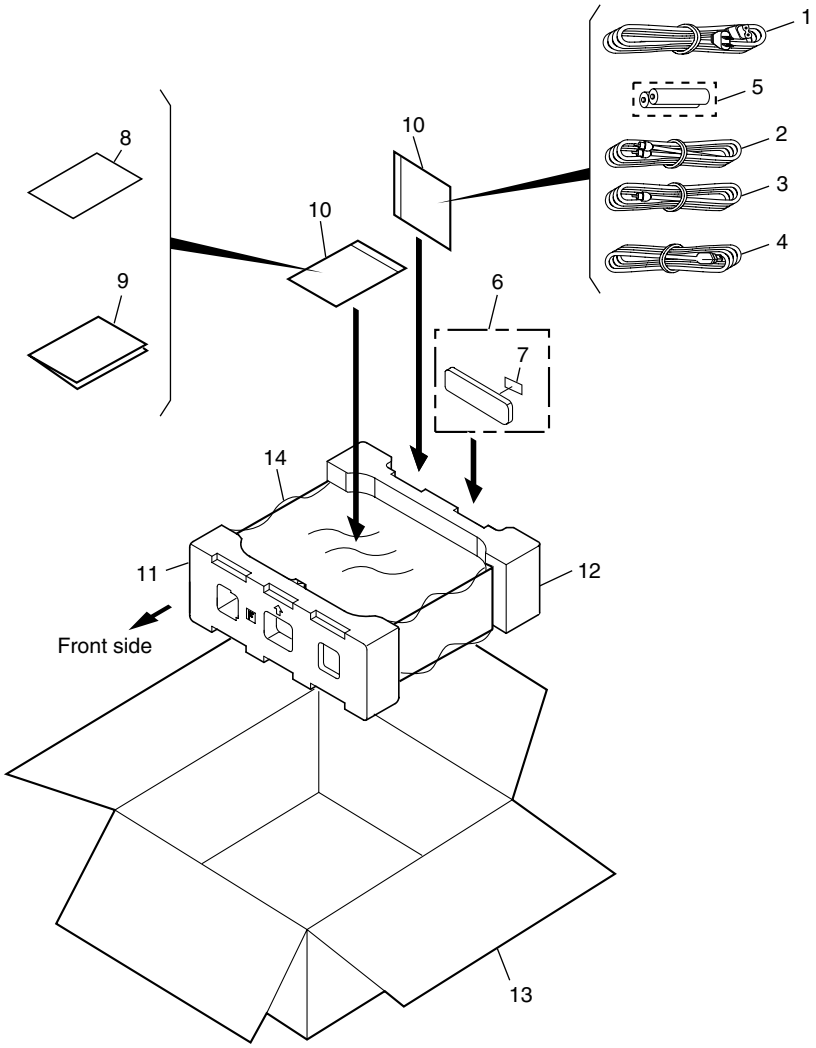
Stereo audio cable 1
Video cable 1
4-pin S400 i.LINK cable 1
Power cable 1
Remote control 1
AA/R6P dry cell batteries 2
Operating Instructions
DV-47Ai 1

Warranty card (DV-47Ai) 1

2. EXPLODED VIEWS AND PARTS LIST

NOTES:
- *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Screws adjacent to ▼ mark on product are used for disassembly.*
- *For the applying amount of lubricants or glue, follow the instructions in this manual. (In the case of no amount instructions, apply as you think it appropriate.)*

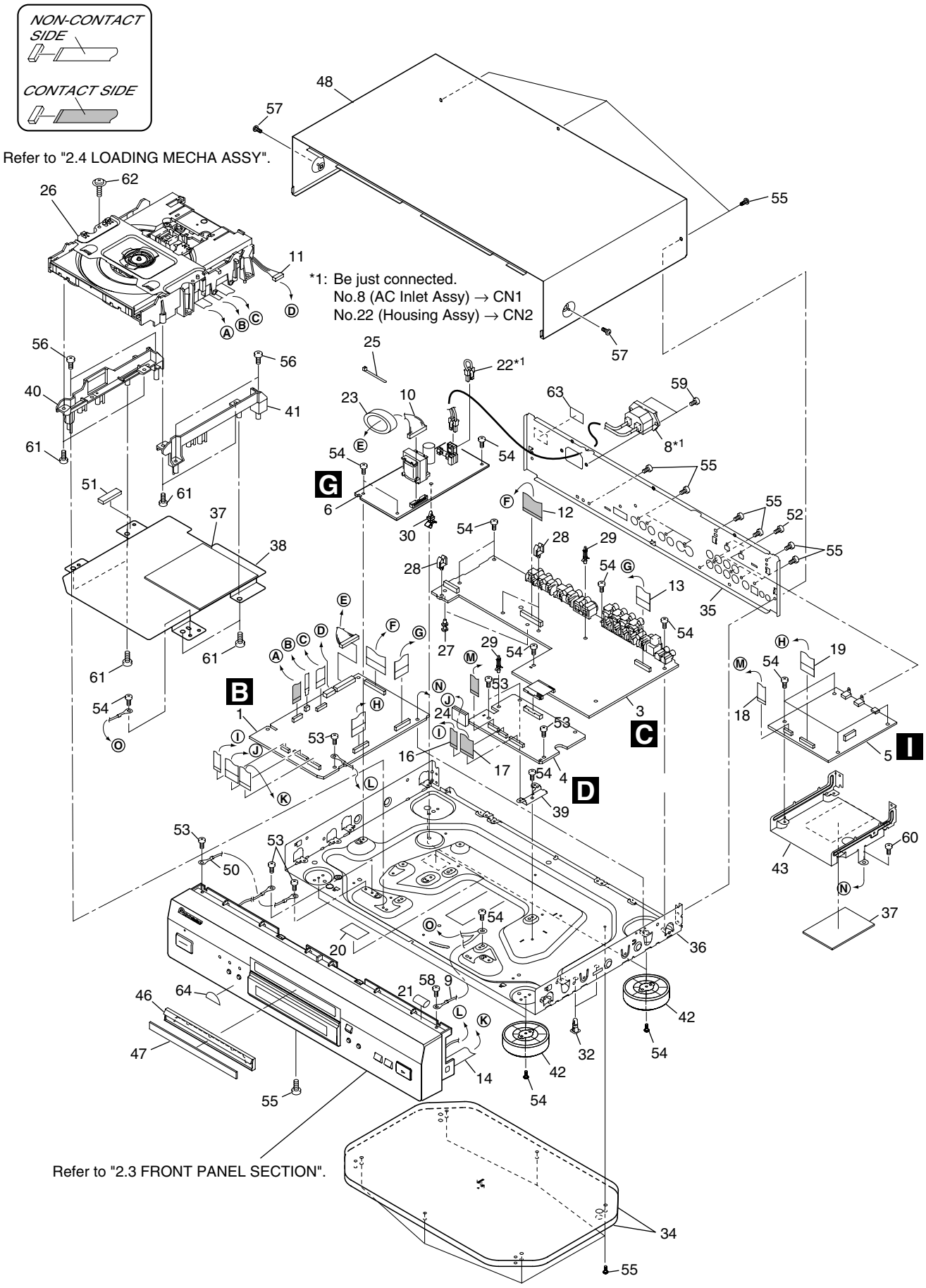
2.1 PACKING



PACKING parts List

Mark	No.	Description	Part No.
⚠	1	Power Cable	ADG7052
	2	Stereo Audio Cable (L = 1.5m)	VDE1052
	3	Video Cable (L = 1.5m)	VDE1053
	4	4-pin S400 i.LINK Cable (L = 1.5m)	VDE1076
NSP	5	AA/R6P Dry Cell Battery	VEM1031
	6	Remote Control	VXX2839
	7	Battery Cover	VNK4423
NSP	8	Warranty Card	ARY7045
	9	Operating Instructions (English)	VRB1299
	10	Polyethylene Bag	VHL1051
	11	Pad F	VHA1311
	12	Pad R	VHA1312
	13	Packing Case	VHG2247
	14	Mirror Mat Sheet	VHL1068

2.2 EXTERIOR SECTION

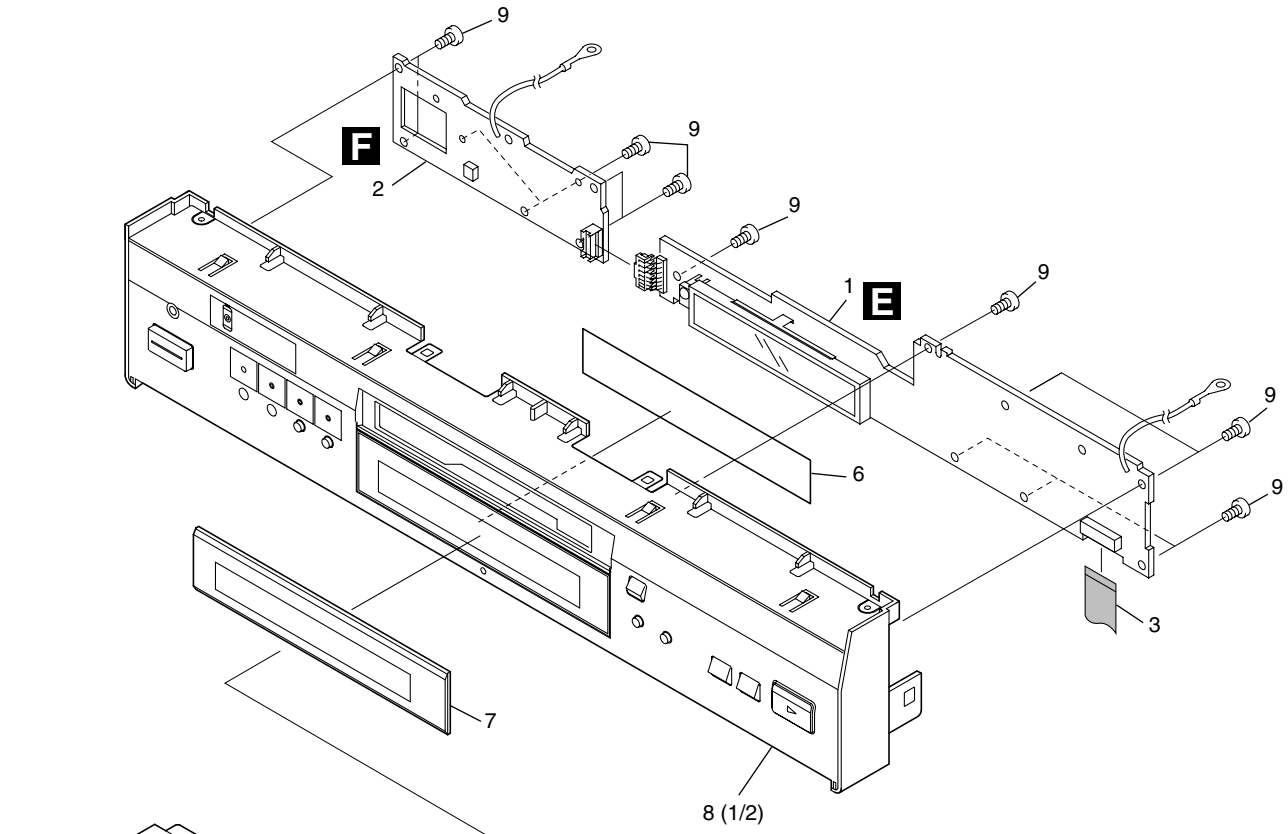


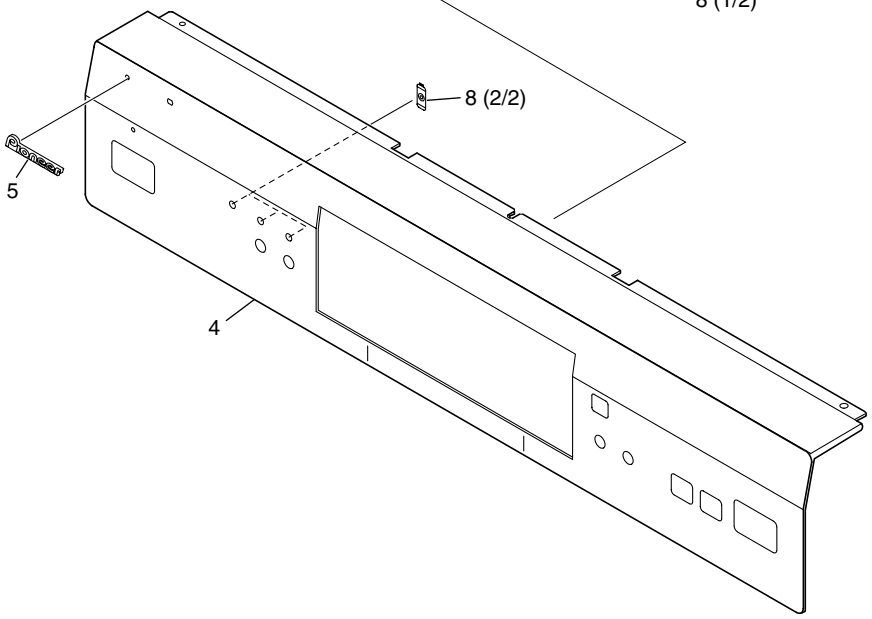
EXTERIOR SECTION parts List

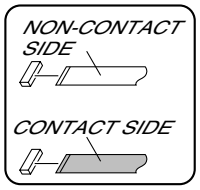
Mark	No.	Description	Part No.
	1	DVDM Assy	VWS1534
	2	•••••	
	3	JACB Assy	VWV1916
	4	SACDB Assy	VWG2353
	5	ILKB Assy	VWG2391
⚠	6	POWER SUPPLY Unit	VWR1361
	7	•••••	
⚠	8	AC Inlet Assy	ADX7406
NSP	9	Earth Lead Unit	VDA1903
	10	Connector Assy	PF13PP-D25
	11	Connector Assy	PG05KK-E30
	12	FFC (30P, JACB)	VDA1905
	13	FFC (21P, JACB)	VDA1906
	14	FFC (17P, FLKB)	VDA1907
	15	•••••	
	16	FFC (20P, DSP)	VDA1909
	17	FFC (40P, SACD)	VDA1910
	18	FFC (13P, ILKB)	VDA1912
	19	FFC (24P, ILKB)	VDA1924
	20	F Cushion	VEB1348
	21	Gasket (6.4X9.5)	VEC2322
⚠	22	Housing Assy	VKP2284
	23	Ferrite Core	VTH1044
	24	Ferrite Core	VTH1045
NSP	25	Binder	ZCA-BK1
NSP	26	01 LOADING MECHA Assy	VWT1203
NSP	27	PCB Spacer (3X6)	AEC7156
	28	Mini Clamp	AEC7373
NSP	29	PCB Support	REC1285
	30	PCB Support	VEC2184
	31	•••••	
	32	PCB Holder	VEC2283
	33	•••••	
NSP	34	Bottom Plate	VNA2469
	35	Rear Panel	VNA2489
NSP	36	Base Chassis	VNA2521
	37	MH Spacer 2	VEC2319
	38	Mechanism Holder	VNE2266
NSP	39	PCB Base	VNE2276
	40	Adapter 27L	VNL1926
	41	Adapter 27R	VNL1927
	42	Insulator	PNW2766
	43	PCB Holder	VNE2280
	44	•••••	
	45	•••••	
	46	Tray Panel	VNK5084
	47	Door	VEC2302
	48	Bonnet S	VXX2846
	49	•••••	
NSP	50	Cord with Plug	DE012VF0

Mark	No.	Description	Part No.
	51	F Cushion 2	VEB1350
	52	Screw	BBZ26P060FZK
	53	Screw	BBZ30P060FCC
	54	Screw	BBZ30P060FMC
	55	Screw	BBZ30P080FZK
	56	Screw	BBZ30P180FMC
	57	Screw	BCZ40P060FZK
	58	Screw	BPZ30P100FMC
	59	Screw	CBZ30P080FZK
	60	Screw	IBZ30P080FCC
	61	Screw	PPZ30P080FMC
	62	Screw	Z39-019
NSP	63	ID Label	VRW1877
NSP	64	Energy Star Label	AAX7876

2.3 FRONT PANEL SECTION







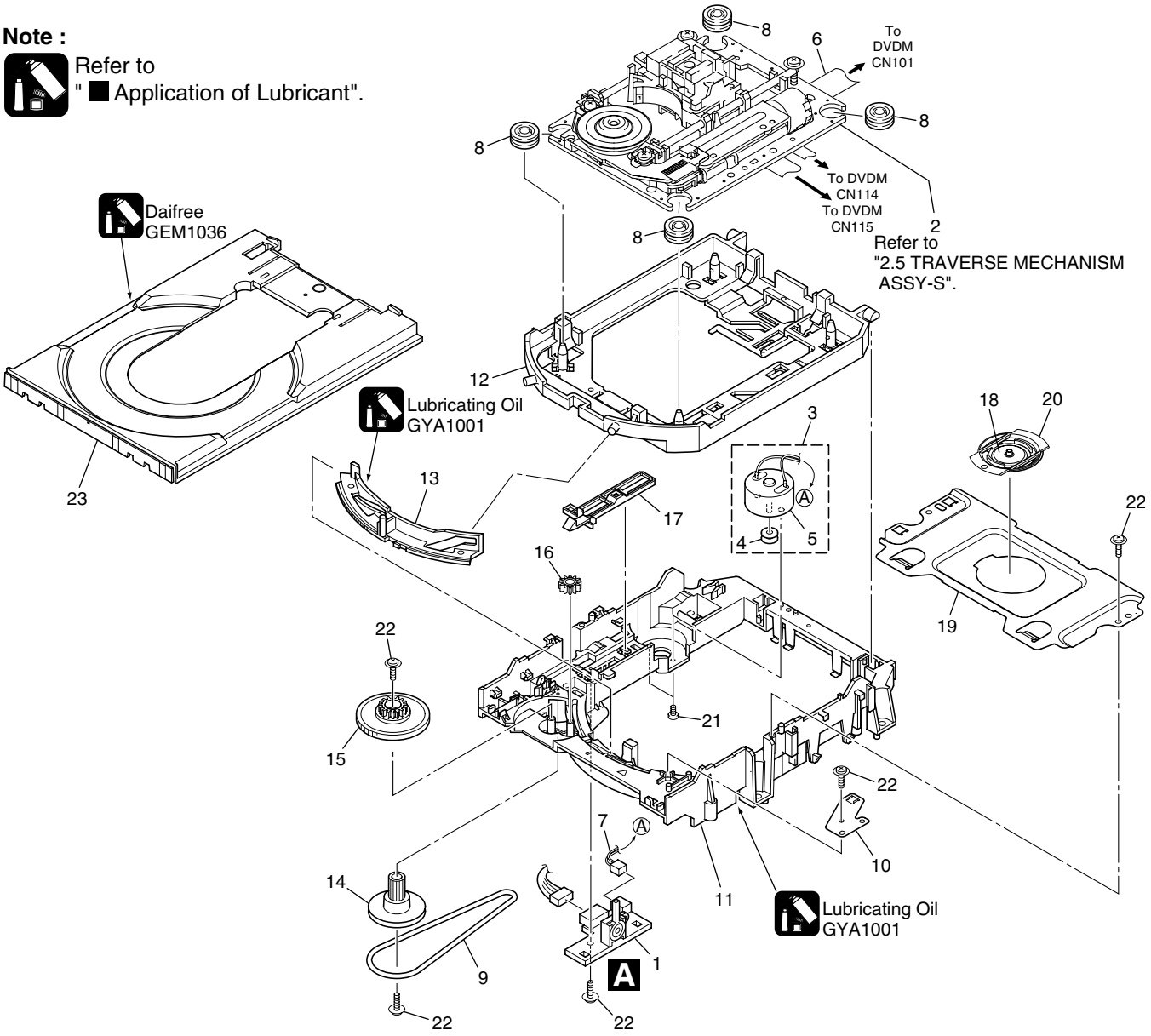
FRONT PANEL SECTION parts List

Mark	No.	Description	Part No.
	1	FLKY Assy	VWG2357
	2	KEYB Assy	VWG2368
	3	FFC (17P, FLKB)	VDA1907
	4	Aluminum Panel	VAH1393
	5	Pioneer Badge	PAN1376
	6	FL Filter	VEC2280
	7	FL Lens	VEC2295
	8	Front Panel Assy	VXA2521
	9	Screw	BBZ30P080FZK

2.4 LOADING MECHA ASSY

Note :

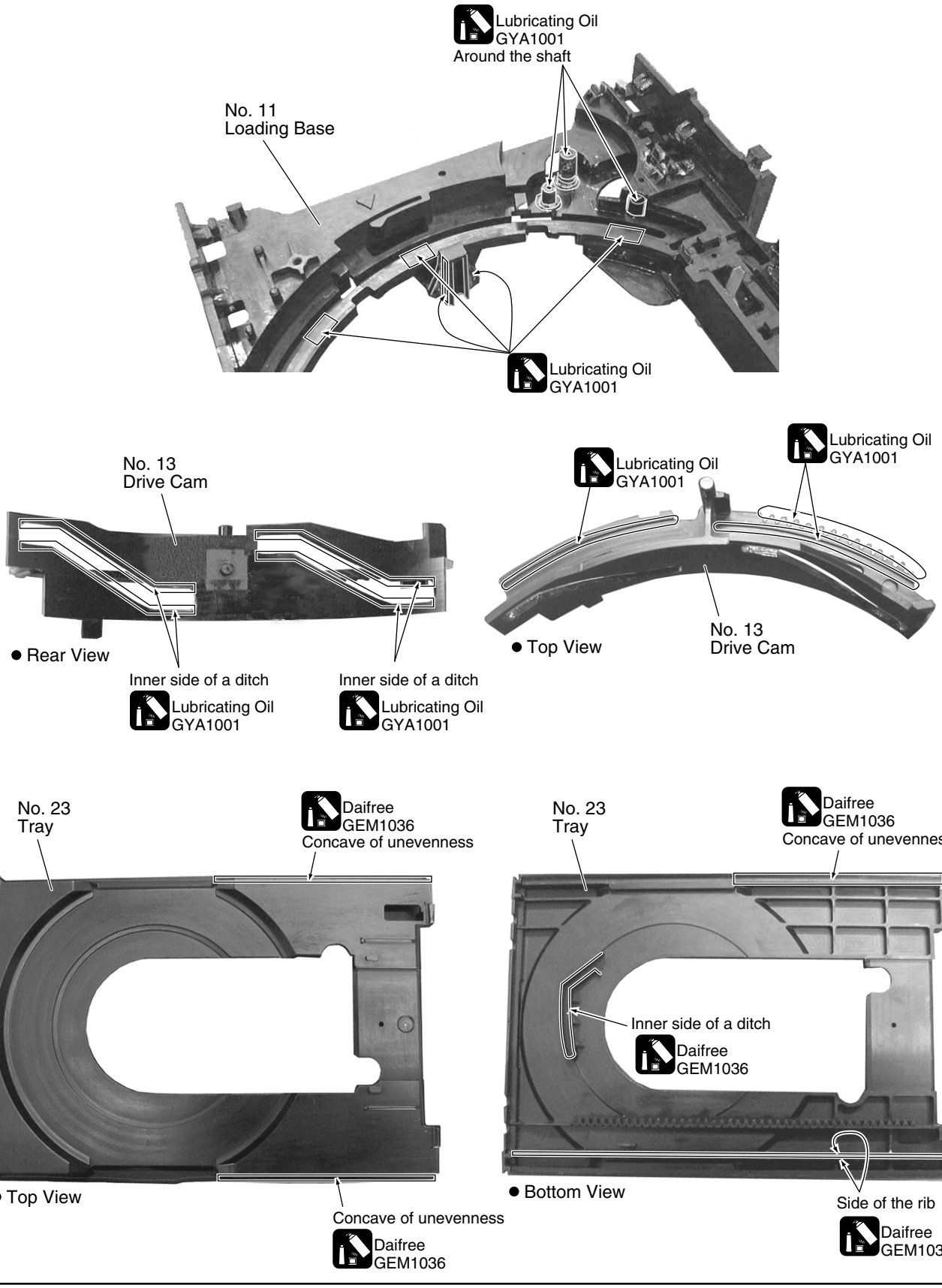
Refer to
" ■ Application of Lubricant".



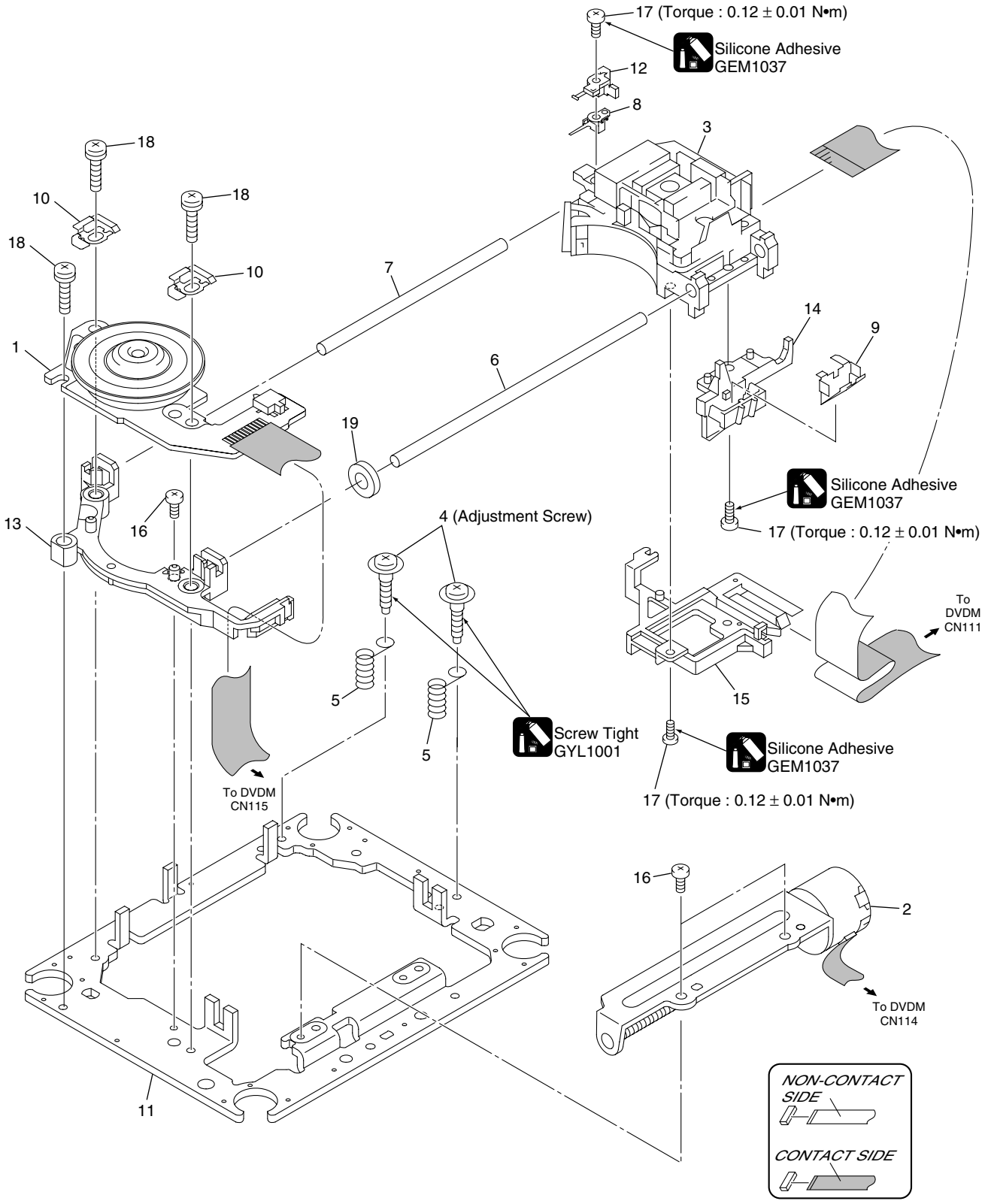
LOADING MECHA ASSY parts List

Mark	No.	Description	Part No.
NSP	1	LOAB Assy	VWG2346
	2	Traverse Mechanism Assy-S	VXX2858
	3	Loading Motor Assy	VXX2505
	4	Motor Pulley	PNW1634
	5	Carriage DC Motor / 0.3W	PXM1027
	6	Flexible Cable (26P)	VDA1864
	7	Connector Assy 2P	VKP2253
	8	Float Rubber	VEB1327
	9	Belt	VEB1330
	10	Stabilizer	VNE2253
	11	Loading Base	VNL1917
	12	Float Base DVD	VNL1918
	13	Drive Cam	VNL1919
	14	Gear Pulley	VNL1921
	15	Loading Gear	VNL1922
	16	Drive Gear	VNL1923
	17	SW Lever	VNL1925
	18	Clamper Plate	VNE2251
	19	Bridge	VNE2252
	20	Clamper	VNL1924
	21	Screw	JGZ17P028FMC
	22	Screw	Z39-019
	23	Tray	VNL1920

Application of Lubricant



2.5 TRAVERSE MECHANISM ASSY-S



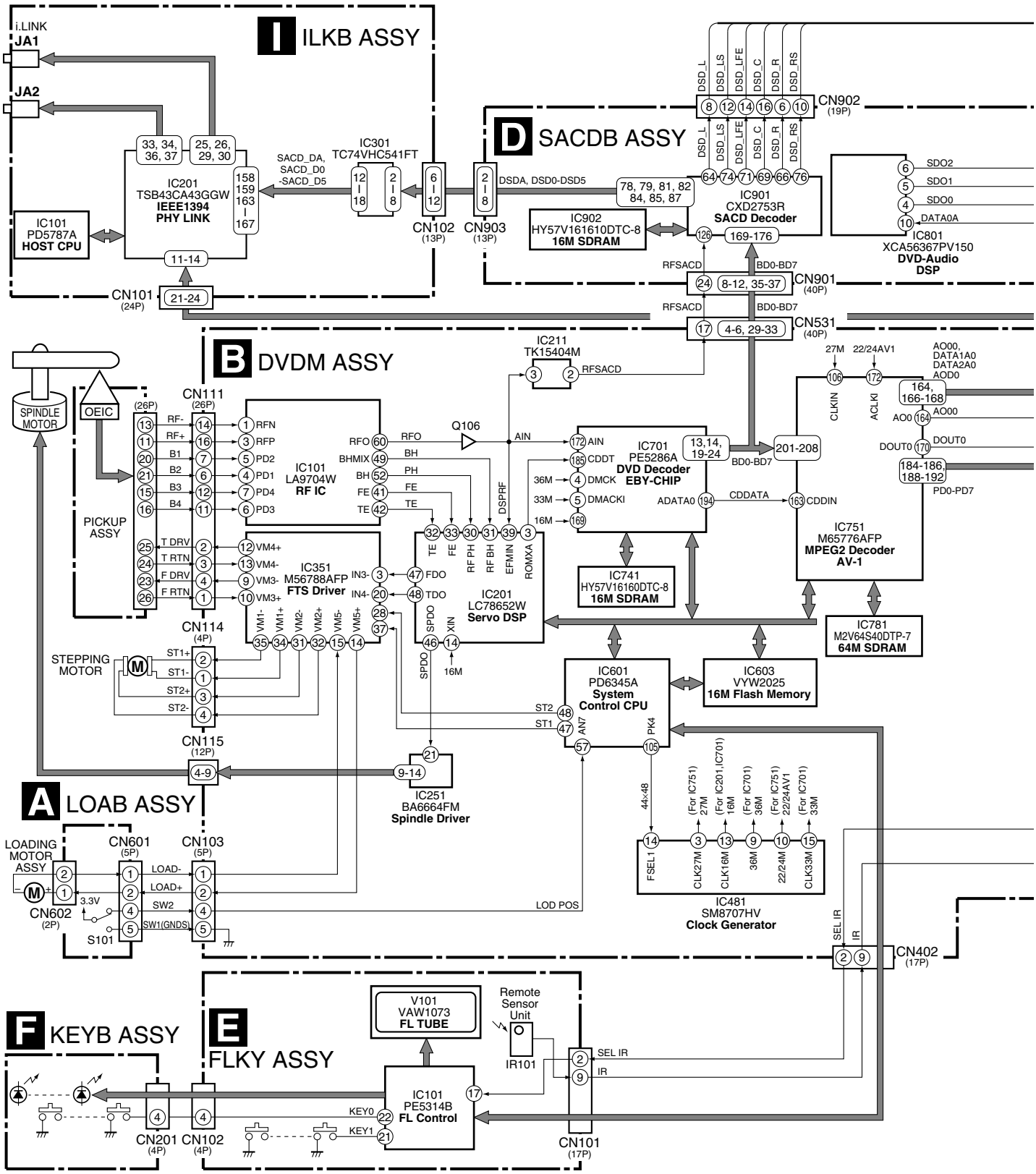
TRAVERSE MECHANISM ASSY-S parts List

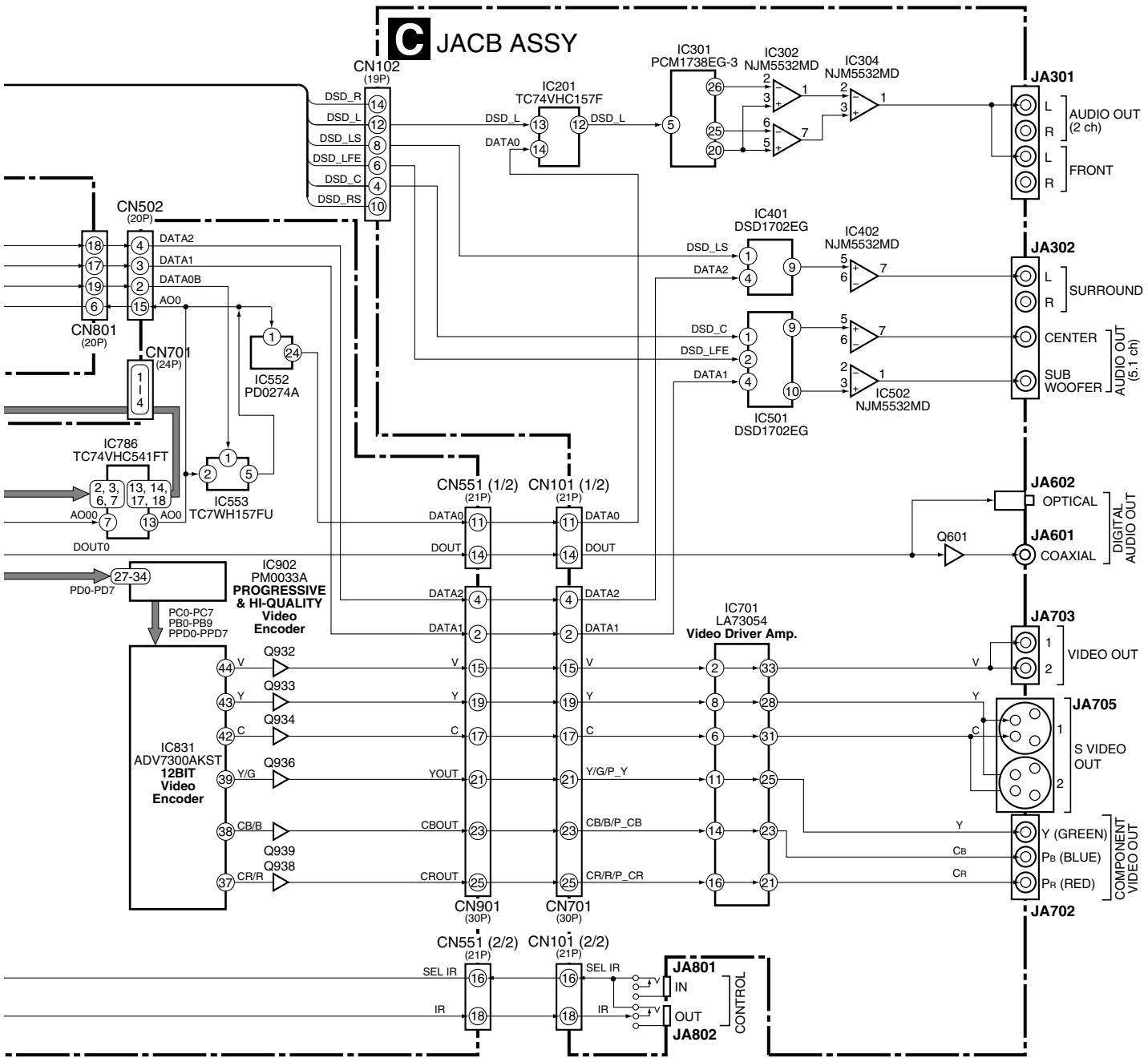
Mark	No.	Description	Part No.
	1	Spindle Motor	VXM1088
	2	Stepping Motor	VXM1090
⚠	3	Pickup Assy-S	OXX8004
	4	Skew Screw	VBA1080
	5	Skew Spring	VBH1335
	6	Guide Bar	VLL1514
	7	Sub Guide Bar	VLL1515
	8	Hold Spring	VNC1017
	9	Joint Spring	VNC1019
	10	Support Spring	VNC1020
NSP	11	Mechanism Chassis	VNE2248
	12	Slider	VNL1811
	13	Spacer	VNL1913
	14	Joint	VNL1914
	15	FFC Holder	VNL1915
	16	Screw	BBZ20P050FZK
	17	Tapping Screw	OBA8009
	18	Screw	PMA26P100FMC
	19	Damper Sheet	VEB1335

3. BLOCK DIAGRAM AND SCHEMATIC DIAGRAM

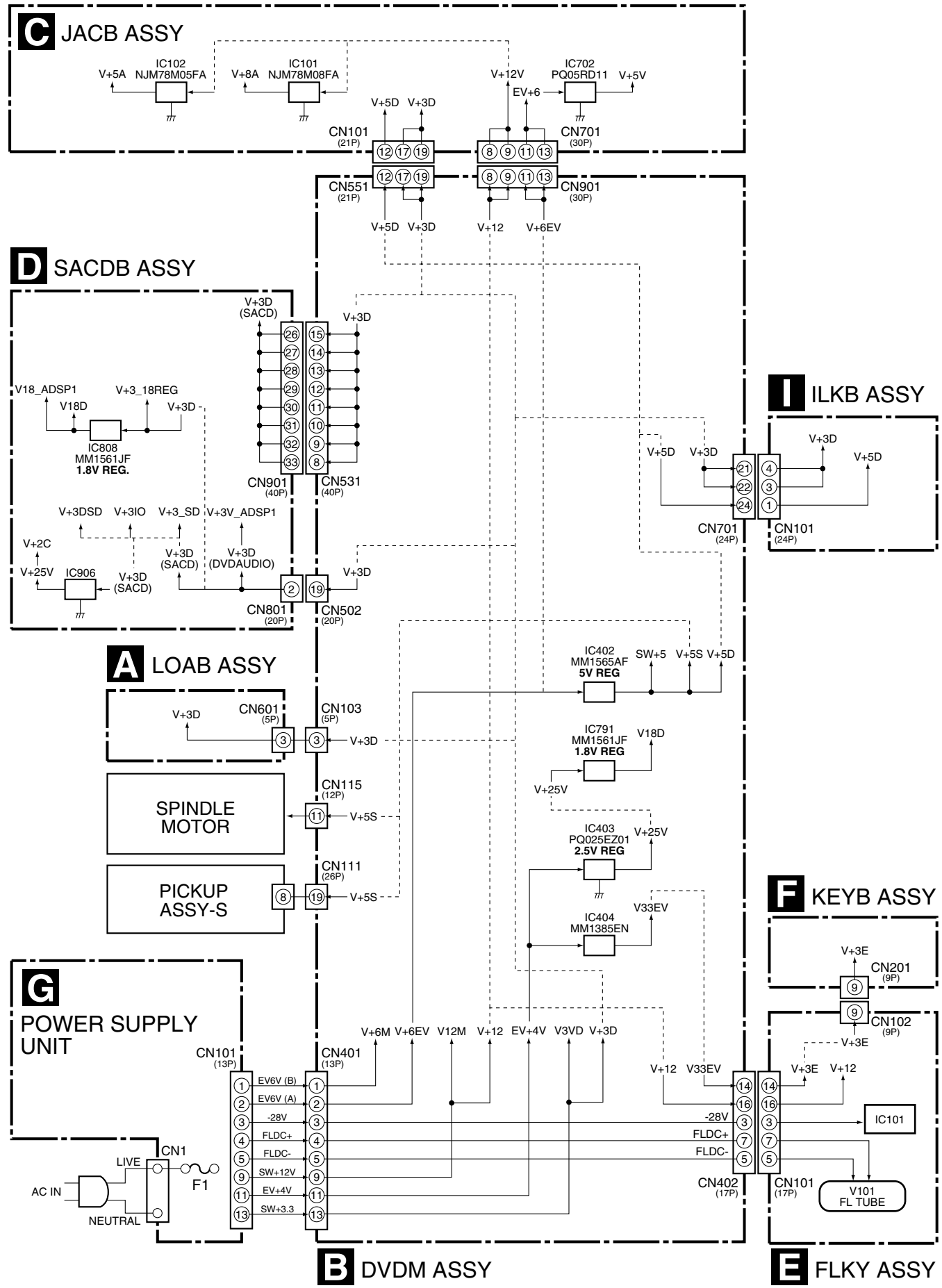
3.1 BLOCK DIAGRAM

■ SIGNAL ROUTE




C JACB ASSY
CN102
(19P)
DSD_R
DSD_L
DSD_LS
DSD_LFE
DSD_C
DSD_RS
IC201
TC74VHC157F
DATA0
IC301
PCM1738EG-3
IC302
NJM5532MD
IC304
NJM5532MD
JA301
L
R
AUDIO OUT
(2 ch)
FRONT
CN502
(20P)
DATA2
DATA1
DATA0B
AO0
CN801
(20P)
CN701
(24P)
IC552
PD0274A
IC401
DSD1702EG
IC402
NJM5532MD
JA302
SURROUND
CENTER
SUB
WOOFER
AUDIO OUT
(5.1 ch)
IC502
NJM5532MD
IC501
DSD1702EG
IC786
TC74VHC541FT
IC553
TC7WH157FU
CN551 (1/2)
(21P)
CN101 (1/2)
(21P)
JA602
OPTICAL
JA601
COAXIAL
DIGITAL
AUDIO OUT
Q601
DOUT0
DOUT
IC902
PM0033A
PROGRESSIVE
& HI-QUALITY
Video
Encoder
PD0-PD7
PC0-PC7
PB0-PB9
PPD0-PPD7
IC701
LA73054
Video Driver Amp.
JA703
VIDEO OUT
Q932
Q933
Q934
Q936
Q939
Q938
IC831
ADV7300AKST
12BIT
Video
Encoder
JA705
S VIDEO
OUT
Y (GREEN)
PB (BLUE)
PR (RED)
COMPONENT
VIDEO OUT
JA702
CN901
(30P)
CN701
(30P)
CN551 (2/2)
(21P)
CN101 (2/2)
(21P)
SEL IR
IR
JA801
IN
OUT
JA802
CONTROL

■ POWER SUPPLY BLOCK



A

B

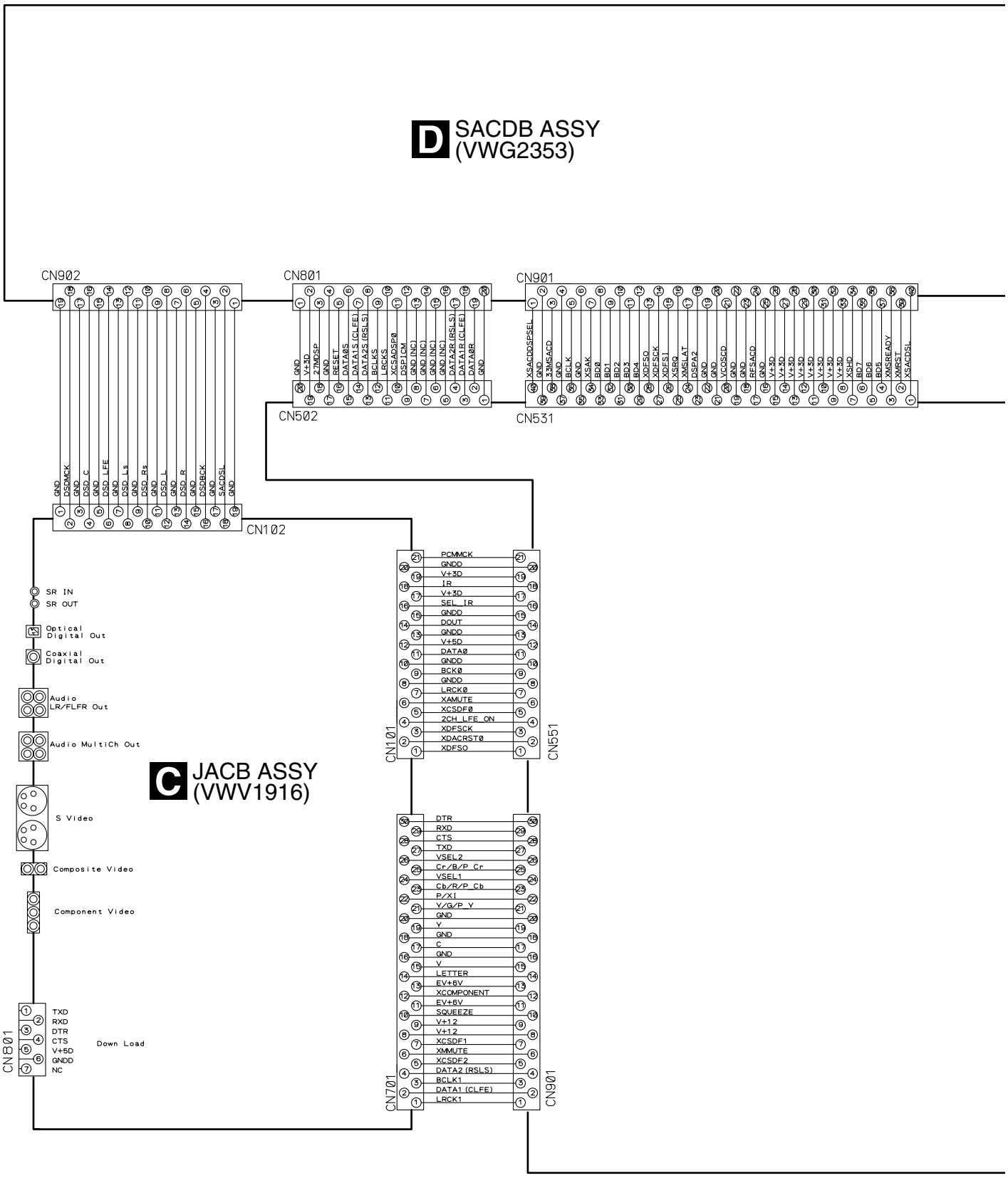
C

D

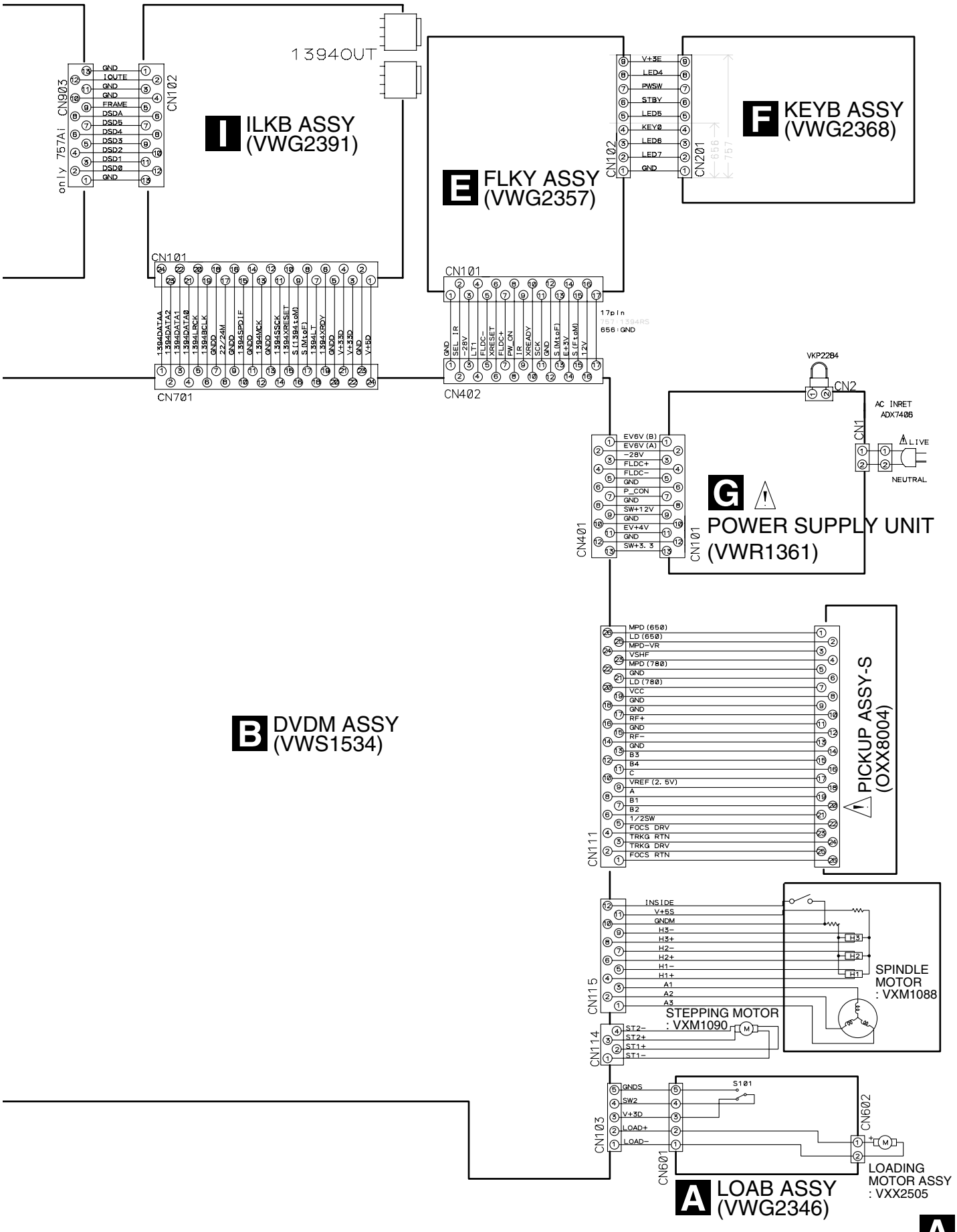
E

F

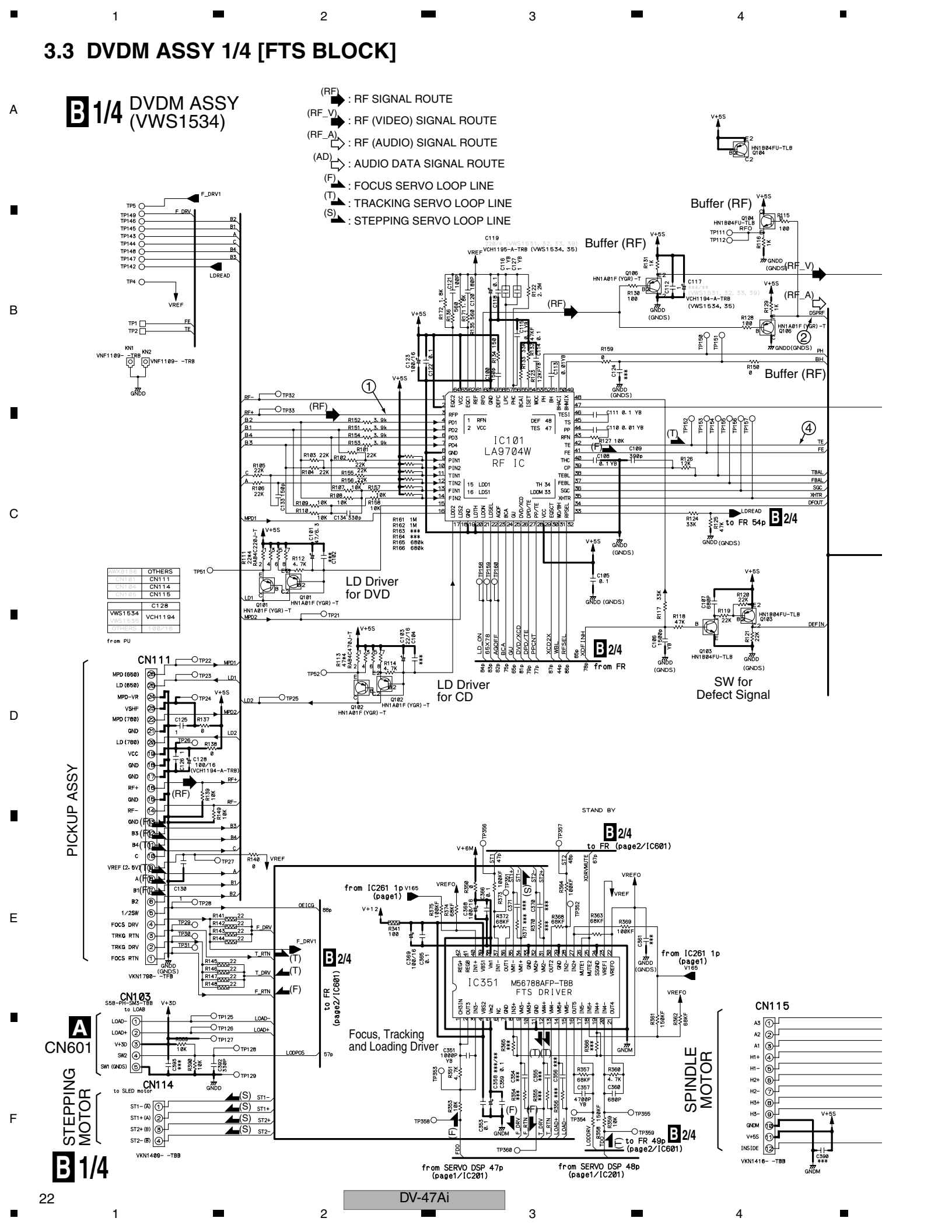
3.2 LOAB ASSY and OVERALL WIRING DIAGRAM

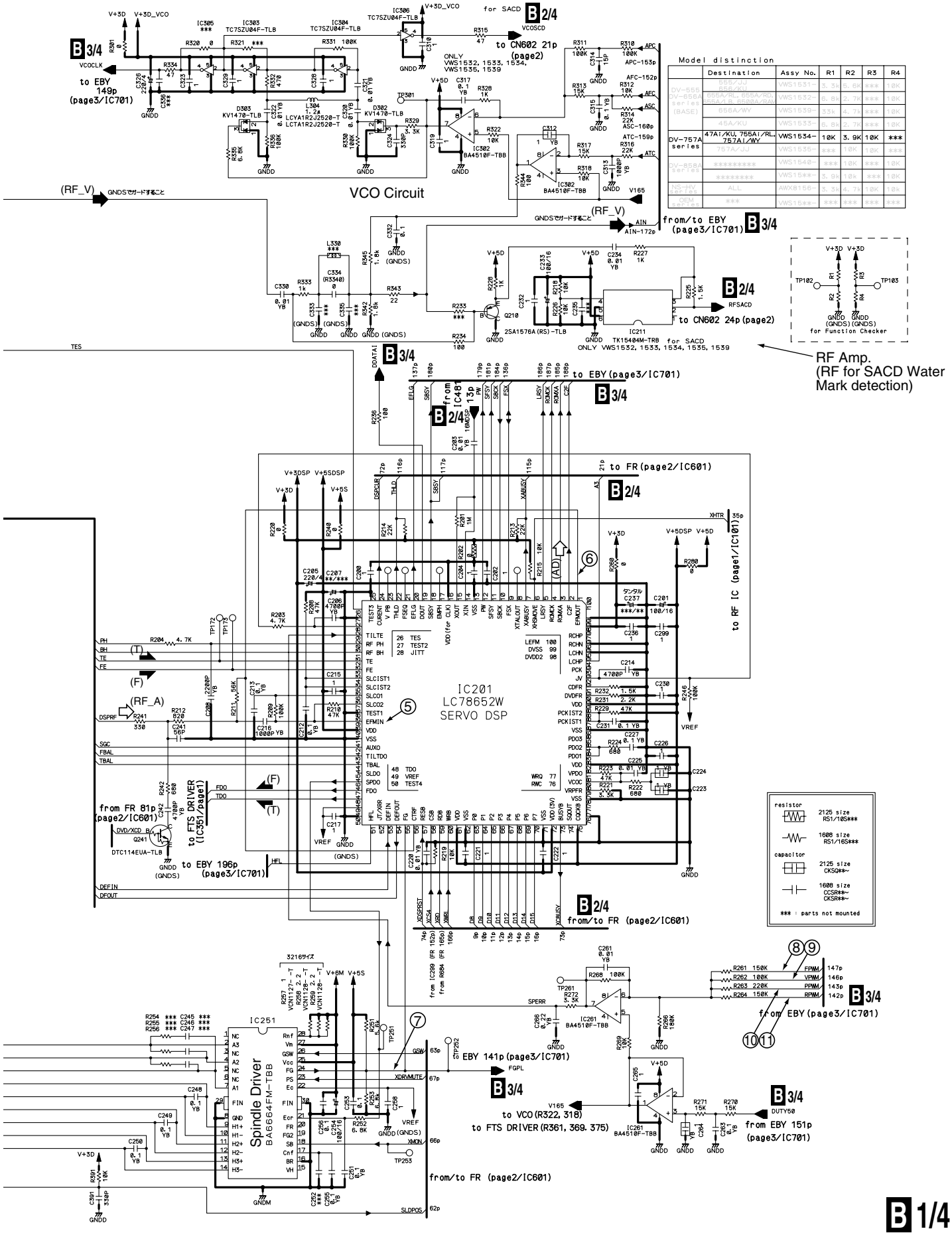


Note : When ordering service parts, be sure to refer to "EXPLODED VIEWS and PARTS LIST" or "PCB PARTS LIST".

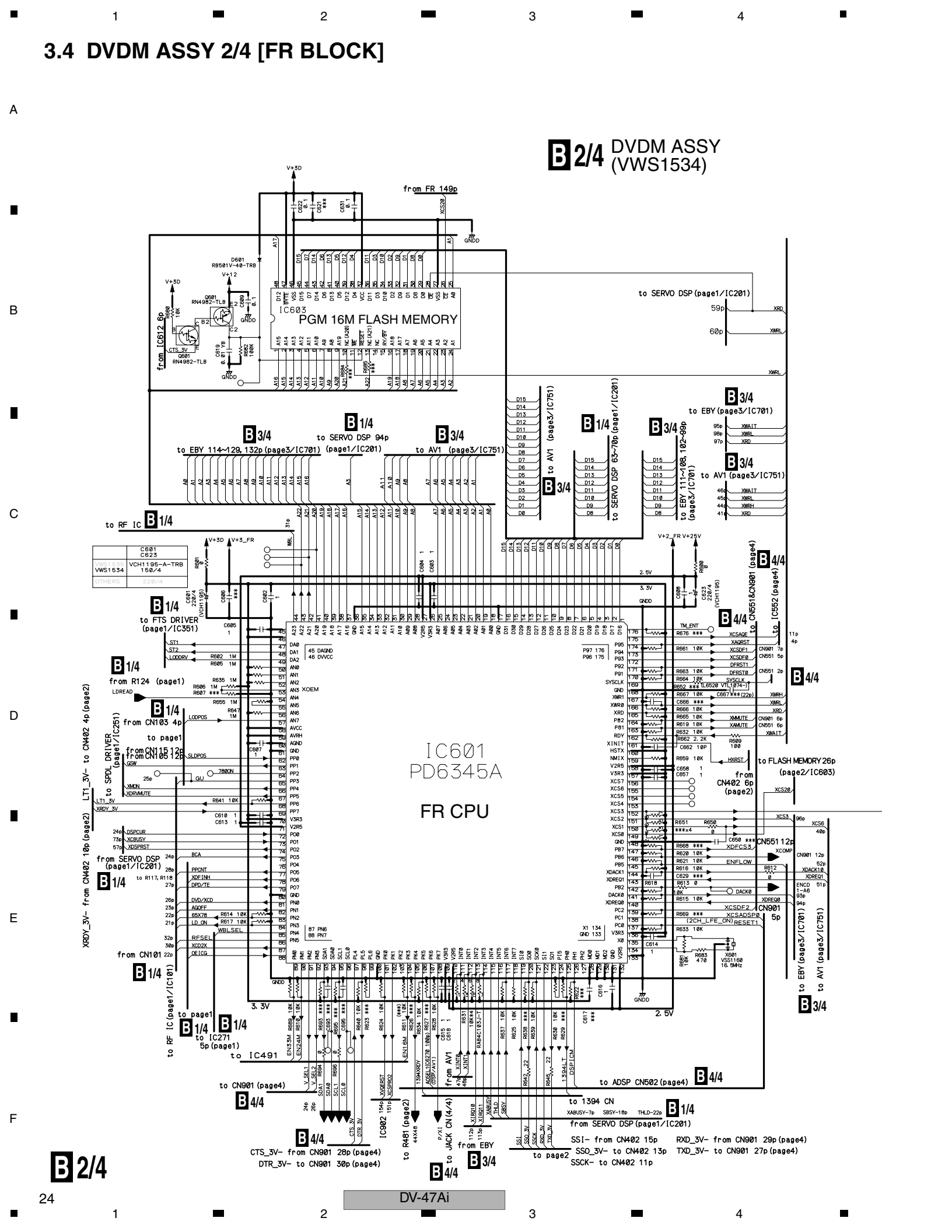

1394OUT
I ILKB ASSY (VWG2391)
E FLKY ASSY (VWG2357)
F KEYB ASSY (VWG2368)
G POWER SUPPLY UNIT (VWR1361)
B DVDM ASSY (VWS1534)
A LOAB ASSY (VWG2346)
PICKUP ASSY-S (OXX8004)
SPINDLE MOTOR : VXM1088
STEPPING MOTOR : VXM1090
LOADING MOTOR ASSY : VXX2505
CN903
CN102
CN101
CN701
CN402
CN201
CN2
CN1
CN401
CN111
CN115
CN114
CN103
CN602
CN601
S101
VKP2284
AC INRET
ADX7406
LIVE
NEUTRAL
only 757Ai
17pin
757:1394RS
656:GND

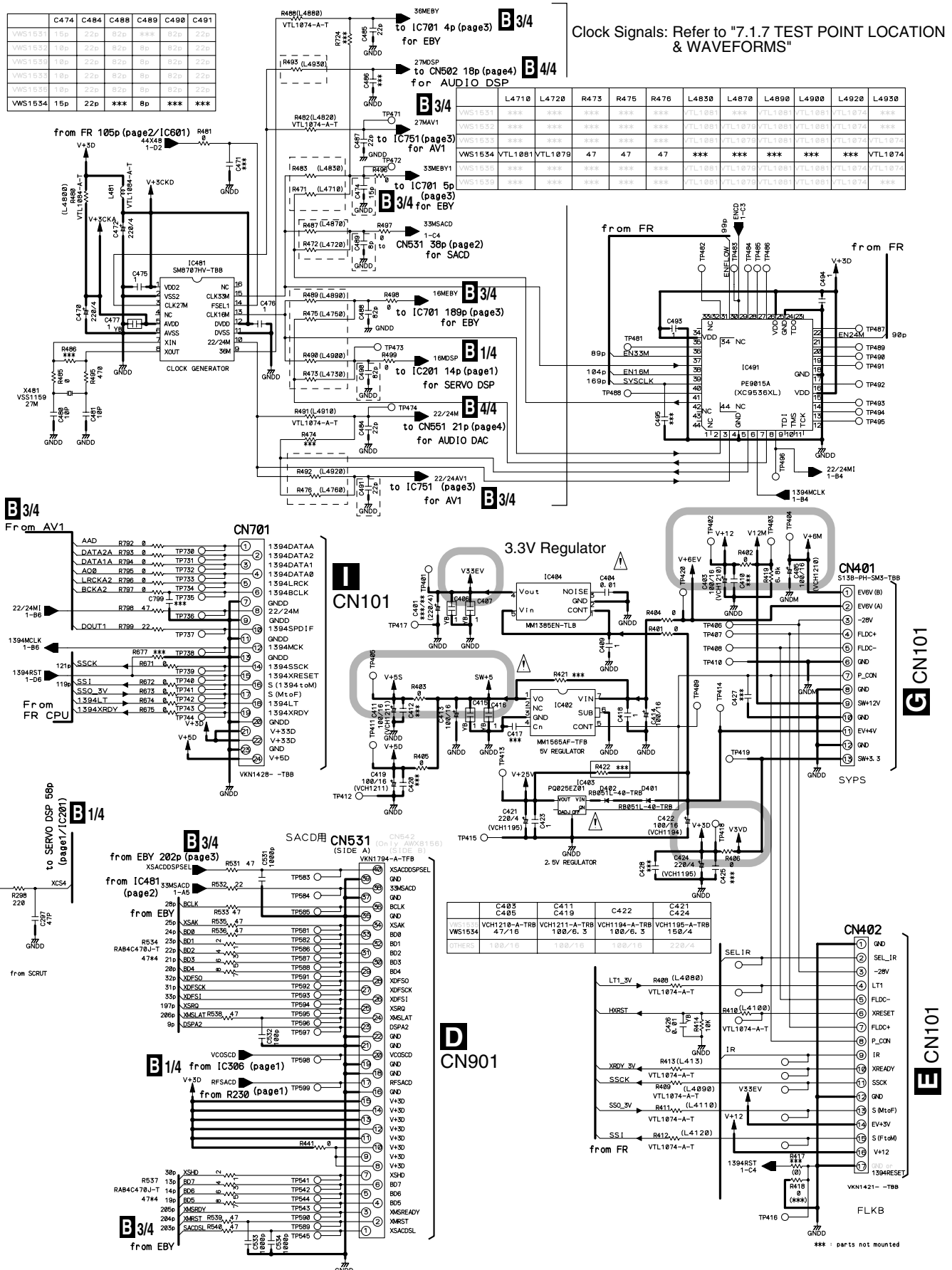
3.3 DVDM ASSY 1/4 [FTS BLOCK]




VCO Circuit
IC201
LC78652W
SERVO DSP
Spindle Driver
BA6664FM-TBB
IC251
RF Amp.
(RF for SACD Water
Mark detection)
Model distinction
Destination
Assy No.
R1
R2
R3
R4
DV-757A series
VWS1534-
10K
3.9K
10K
***
DV-555 series
DV-656A series
DV-858A series
NS-HV series
OEM series
ALL
AWX8156-
VWS15**-
resistor
2125 size RS1/10S***
1608 size RS1/16S***
capacitor
2125 size CKSQ***-
1608 size CCSR**-
CKSR**-
*** : parts not mounted
from/to EBY (page3/IC701) B 3/4
to EBY 149p (page3/IC701)
to CN602 21p (page2)
to CN602 24p (page2)
RFSACD
from/to FR (page2/IC601) B 2/4
to FR (page2/IC601)
to RF IC (page1/IC101)
to EBY (page3/IC701)
from IC481 13p
from FR 81p (page2/IC601)
to FTS DRIVER (IC351/page1)
to EBY 196p (page3/IC701)
from EBY (page3/IC701)
to EBY 141p (page3/IC701)
to VCO (R322, 318)
to FTS DRIVER (R361, 369, 375)
from EBY 151p (page3/IC701)
from/to FR (page2/IC601)
for SACD
ONLY VWS1532, 1533, 1534, VWS1535, 1539
ONLY VWS1532, 1533, 1534, 1535, 1539
for Function Checker
B 1/4

3.4 DVDM ASSY 2/4 [FR BLOCK]





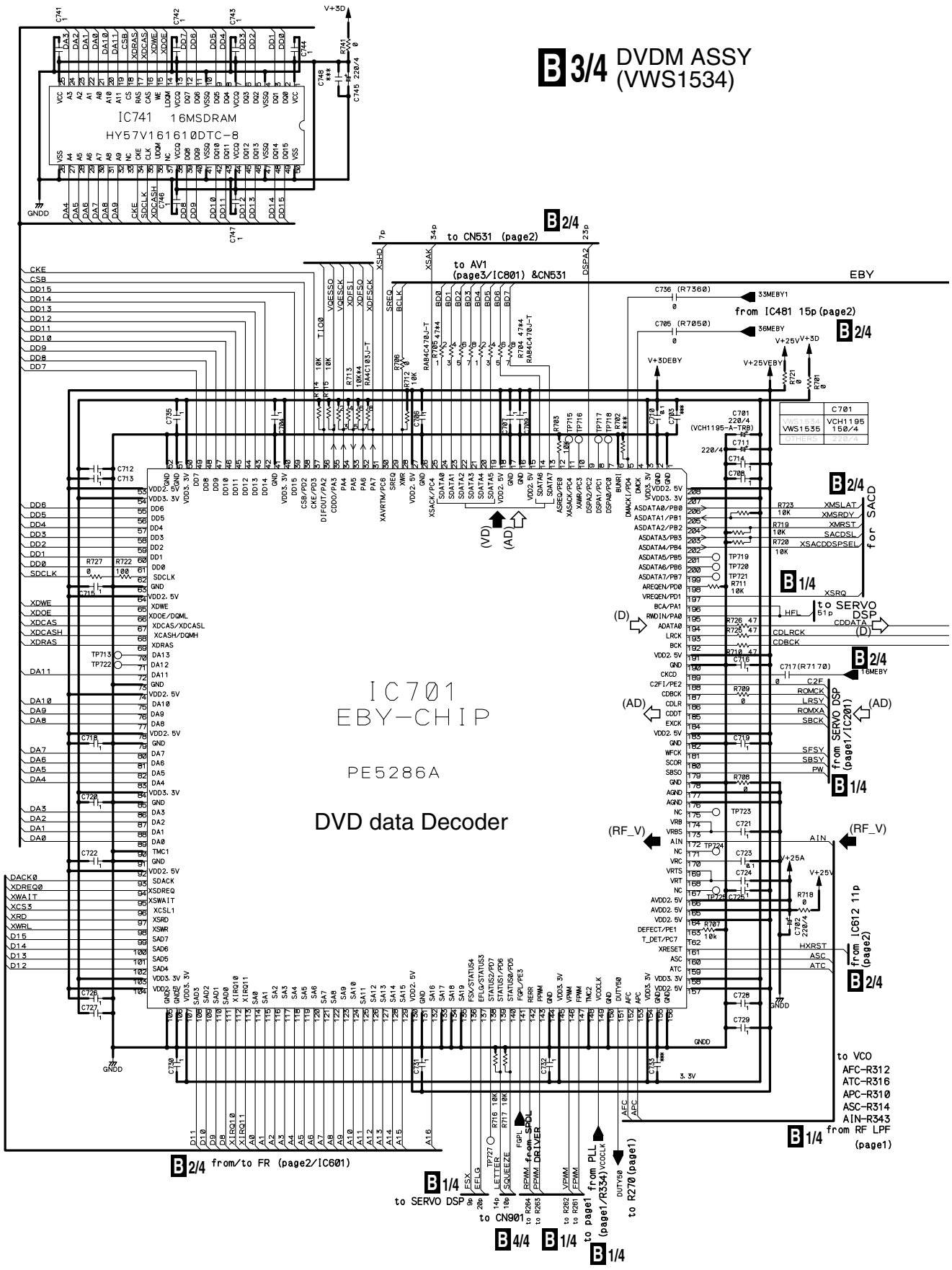
	C474	C484	C488	C489	C490	C491
VWS1531	15p	22p	82p	***	82p	22p
VWS1532	10p	22p	82p	8p	82p	22p
VWS1533	10p	22p	82p	8p	82p	22p
VWS1537	10p	22p	82p	8p	82p	22p
VWS1538	10p	22p	82p	8p	82p	22p
VWS1534	15p	22p	***	8p	***	***

	L4710	L4720	R473	R475	R476	L4830	L4870	L4890	L4900	L4920	L4930
VWS1531	***	***	***	***	***	VTL1081	***	VTL1081	VTL1081	VTL1074	***
VWS1532	***	***	***	***	***	VTL1081	VTL1079	VTL1081	VTL1081	VTL1074	***
VWS1533	***	***	***	***	***	VTL1081	VTL1079	VTL1081	VTL1081	VTL1074	VTL1074
VWS1534	VTL1081	VTL1079	47	47	47	***	***	***	***	***	VTL1074
VWS1535	***	***	***	***	***	VTL1081	VTL1079	VTL1081	VTL1081	VTL1074	VTL1074
VWS1539	***	***	***	***	***	VTL1081	VTL1079	VTL1081	VTL1081	VTL1074	***

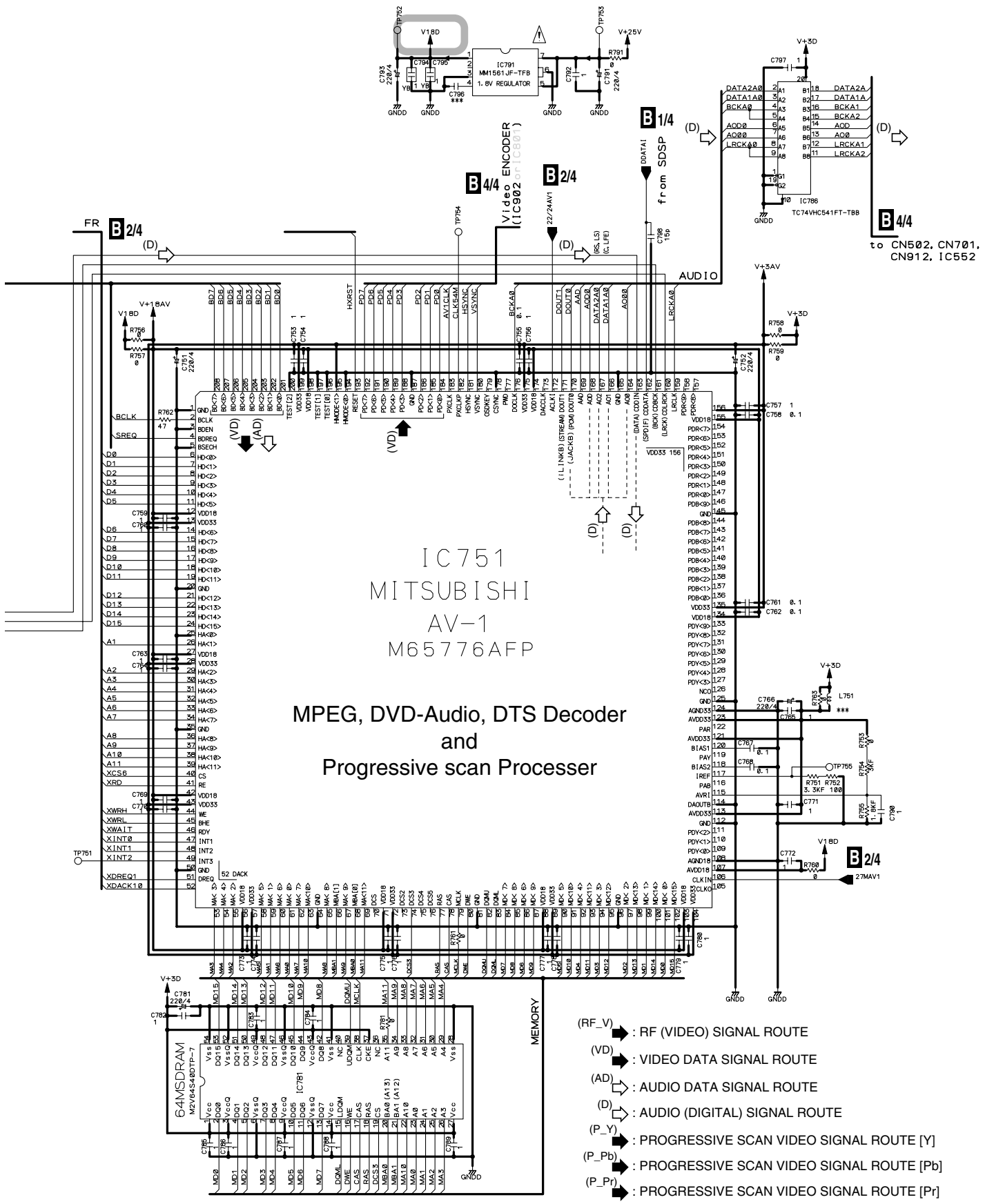
	C403 C405	C411 C419	C422	C421 C424
VWS1531	VCH1210-A-TRB	VCH1211-A-TRB	VCH1194-A-TRB	VCH1195-A-TRB
VWS1534	47/16	100/6.3	100/6.3	150/4
OTHERS	100/16	100/16	100/16	220/4

*** : parts not mounted

3.5 DVDM ASSY 3/4 [EBY/AV1 BLOCK]

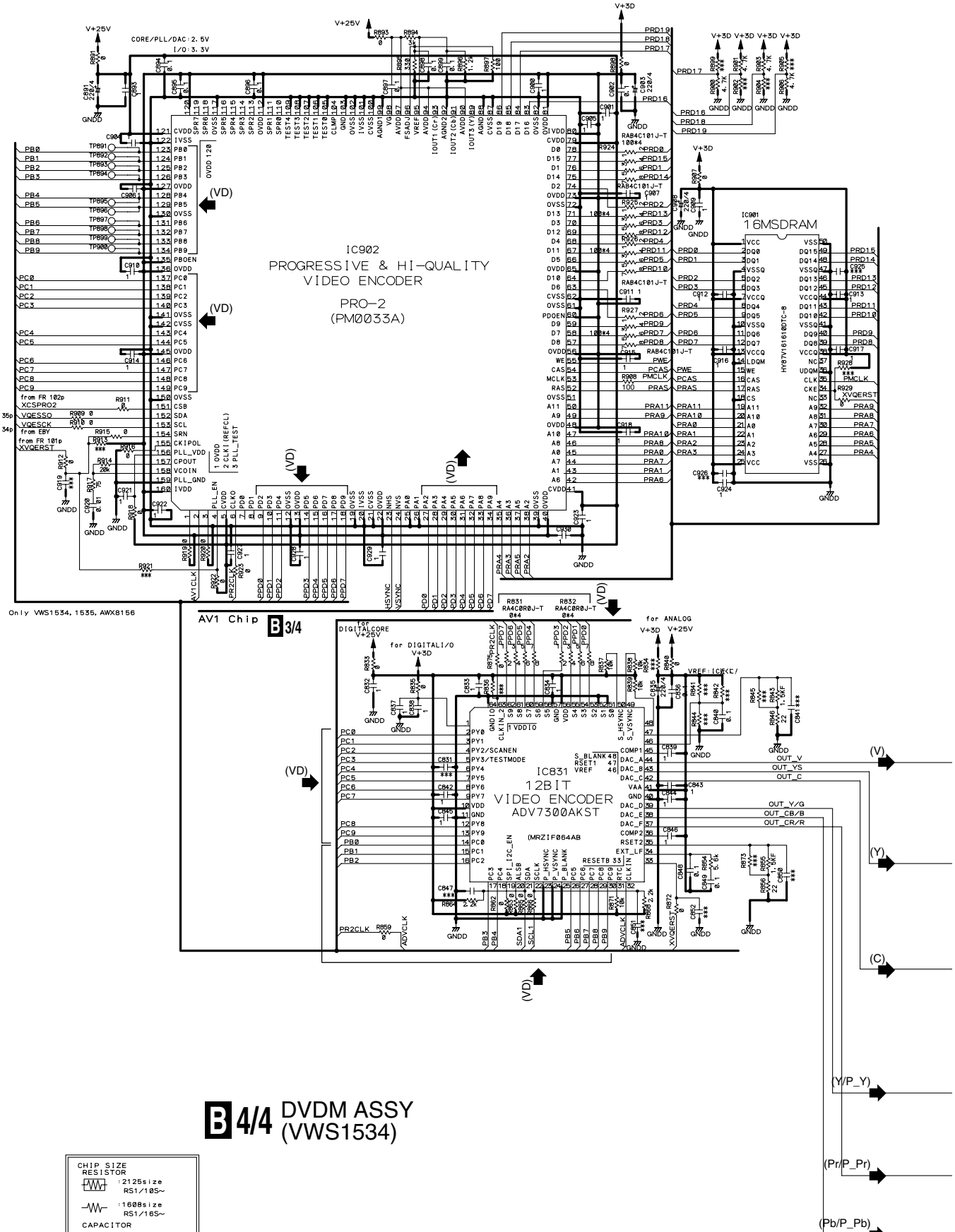


: The power supply is shown with the marked box.



B 3/4

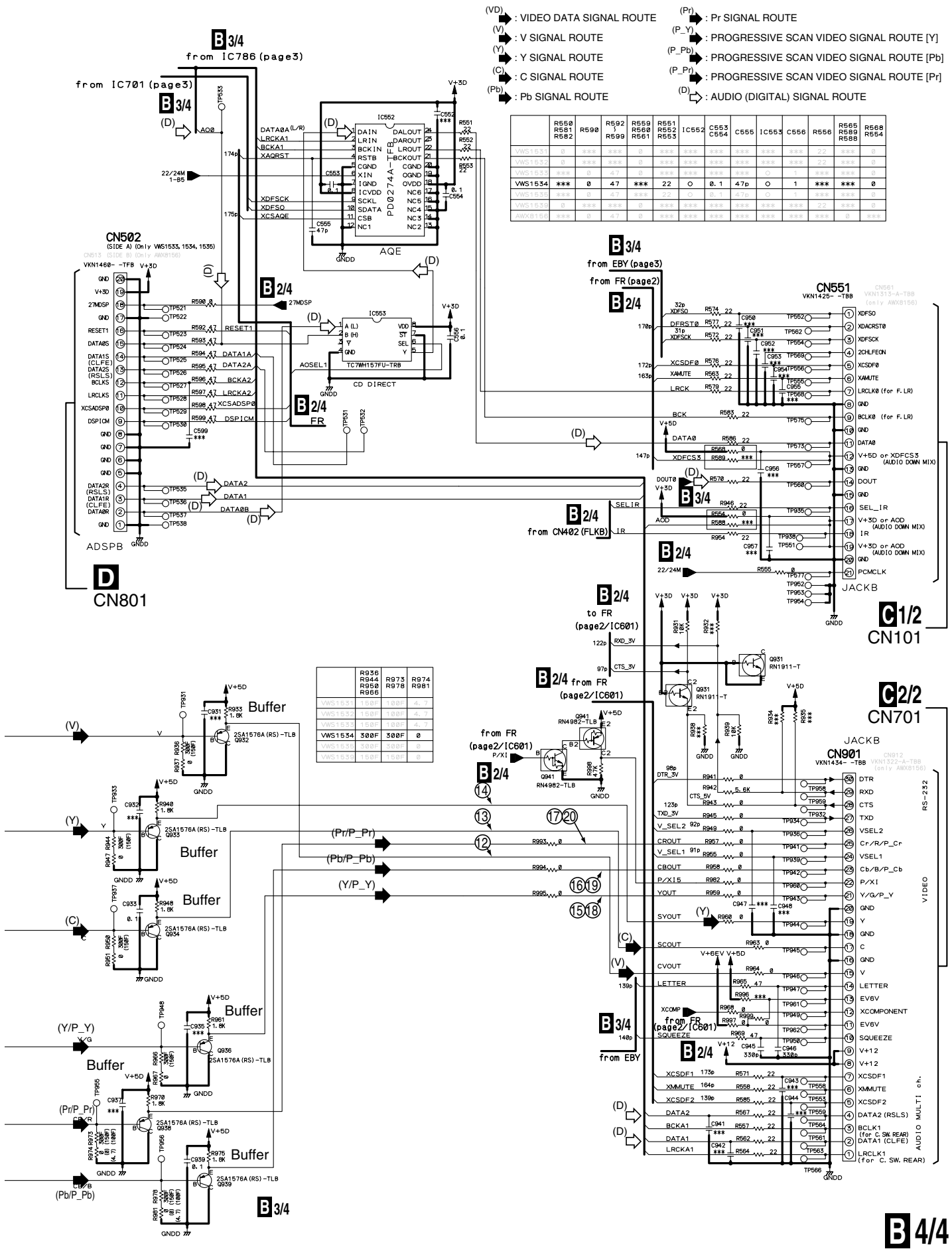
3.6 DVDM ASSY 4/4 [VENC BLOCK]



B 4/4 DVDM ASSY (VWS1534)

CHIP SIZE
RESISTOR
:2125size RS1/10S~
:1608size RS1/16S~
CAPACITOR
:2125size CKSQ**~
:1608size CCSR**~ or CKSR**~

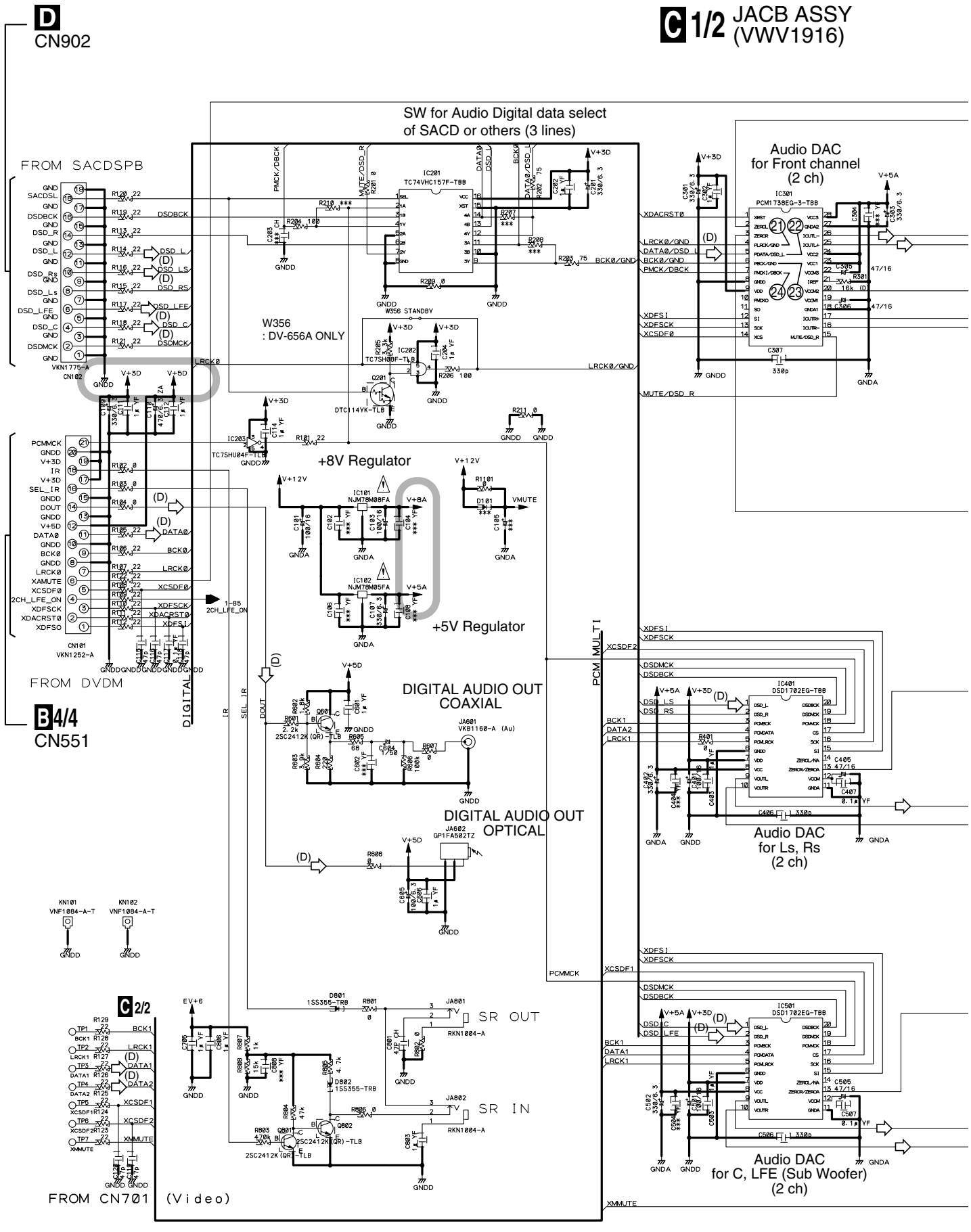
B 4/4



	R550 R581 R582	R590	R592) R599	R559 R560 R561	R551 R552 R553	IC552	C553 C554	C555	IC553	C556	R556	R565 R589 R588	R568 R554
VWS1531	0	***	***	0	***	***	***	***	***	***	22	***	0
VWS1532	0	***	***	0	***	***	***	***	***	***	22	***	0
VWS1533	***	0	47	0	***	***	***	***	○	1	***	***	0
VWS1534	***	0	47	***	22	○	0.1	47p	○	1	***	***	0
VWS1535	***	0	47	***	22	○	0.1	47p	○	1	***	***	0
VWS1536	0	***	***	0	***	***	***	***	***	***	22	***	0
AWX8156	***	0	47	0	***	***	***	***	***	***	***	0	***

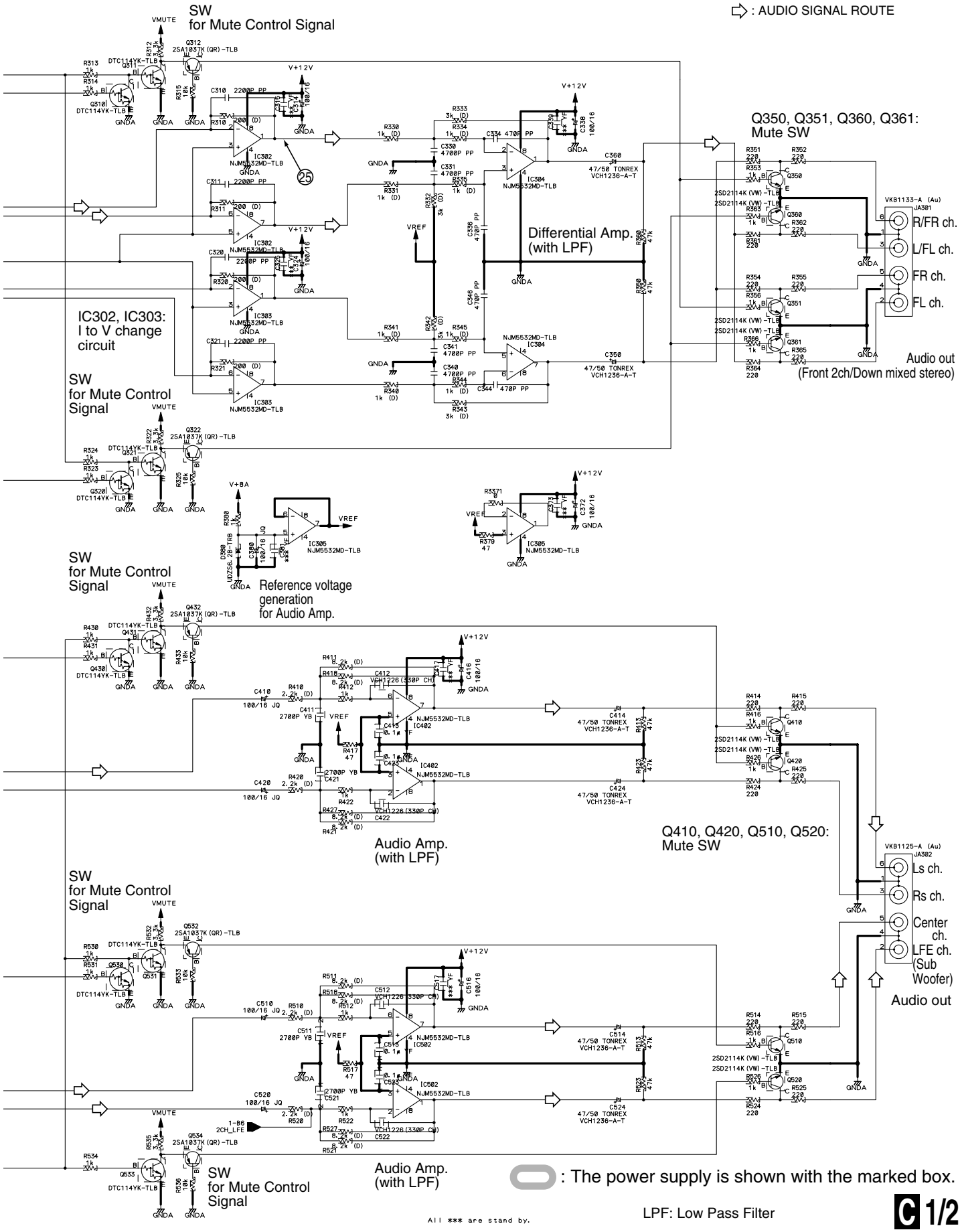
	R936 R944 R950 R956	R973 R978	R974 R981
VWS1531	150F	100F	4.7
VWS1532	150F	100F	4.7
VWS1533	150F	100F	4.7
VWS1534	300F	300F	0
VWS1535	300F	300F	0
VWS1536	150F	150F	0

3.7 JACB ASSY 1/2 [AUDIO BLOCK]



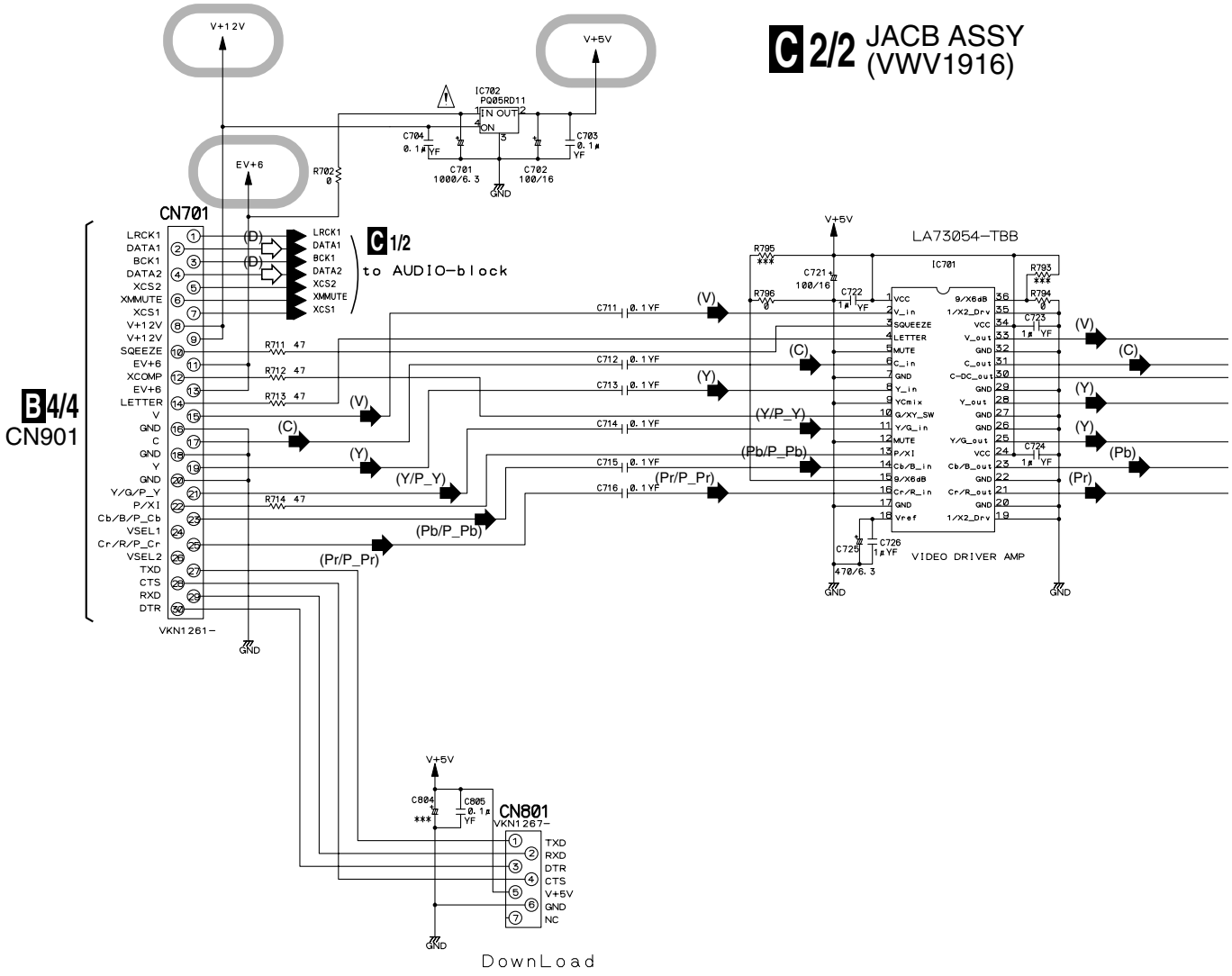
(D) ⇨ : AUDIO (DIGITAL) SIGNAL ROUTE

⇨ : AUDIO SIGNAL ROUTE



C 1/2

3.8 JACB ASSY 2/2 [VIDEO BLOCK]



(V) : V SIGNAL ROUTE

(Y) : Y SIGNAL ROUTE

(C) : C SIGNAL ROUTE

(Pb) : Pb SIGNAL ROUTE

(Pr) : Pr SIGNAL ROUTE

(P_Y) : PROGRESSIVE SCAN VIDEO SIGNAL ROUTE [Y]

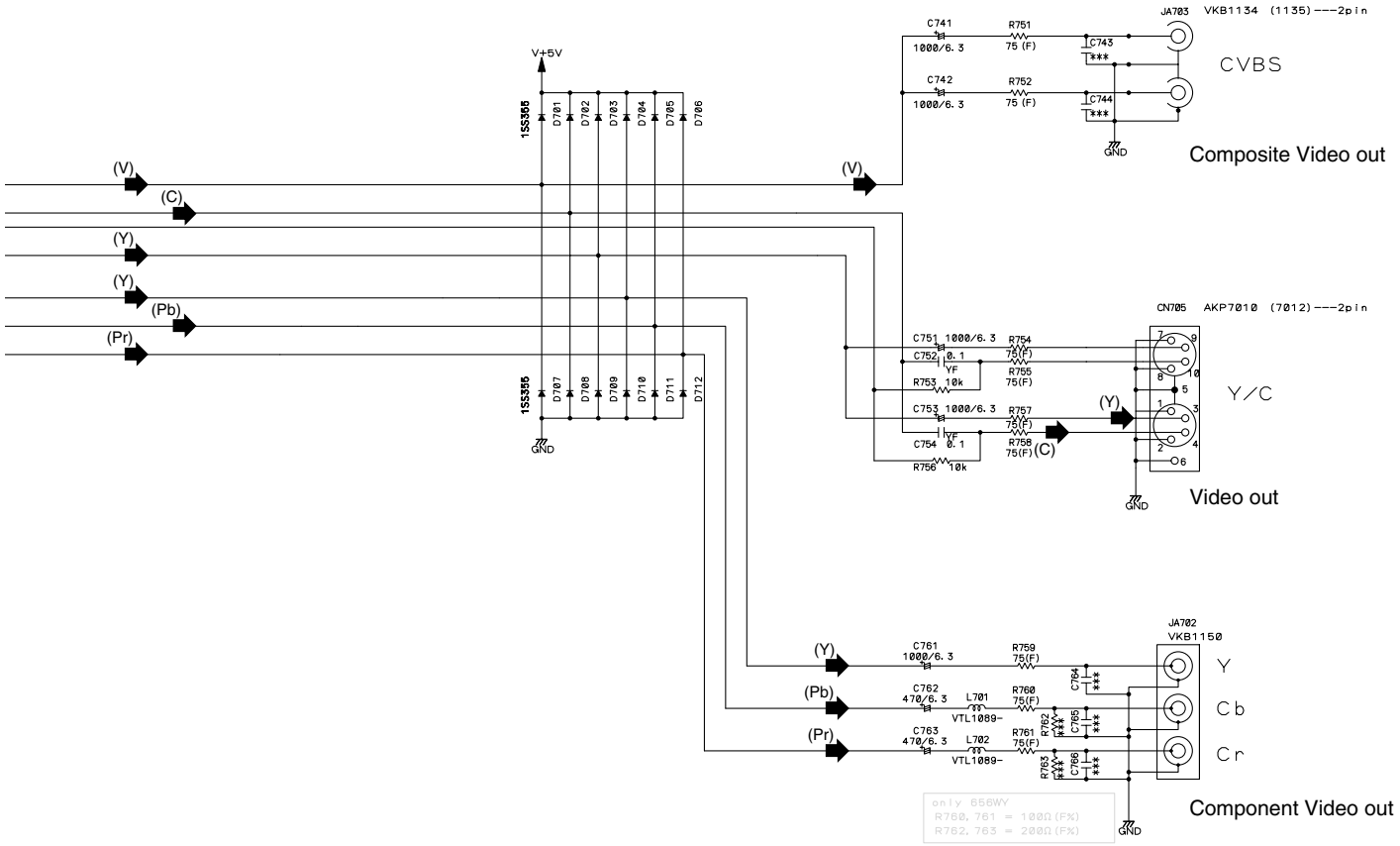
(P_Pb) : PROGRESSIVE SCAN VIDEO SIGNAL ROUTE [Pb]

(P_Pr) : PROGRESSIVE SCAN VIDEO SIGNAL ROUTE [Pr]

(D) : AUDIO (DIGITAL) SIGNAL ROUTE

C 2/2

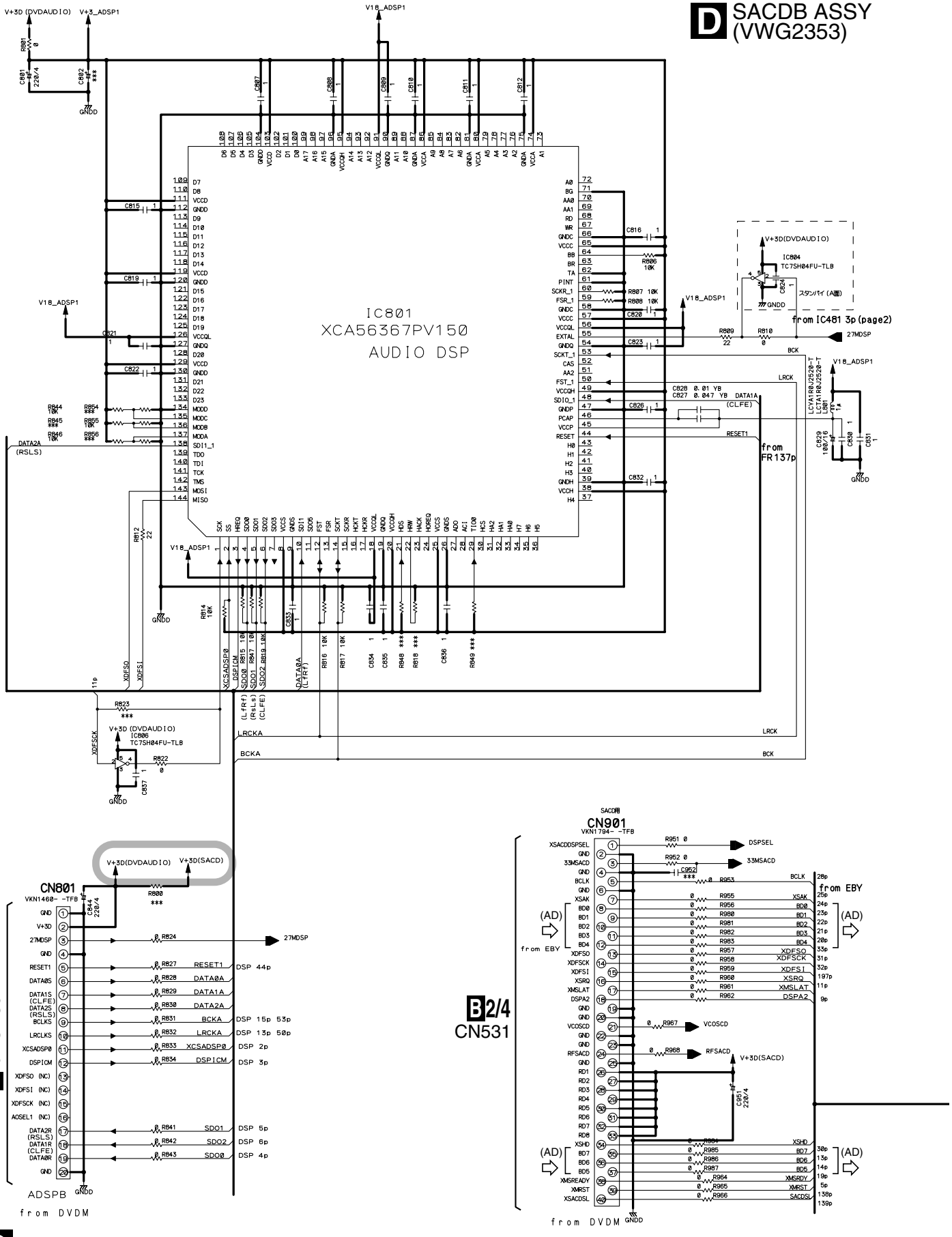
: The power supply is shown with the marked box.



All *** are stand by.

C 2/2

3.9 SACDB ASSY

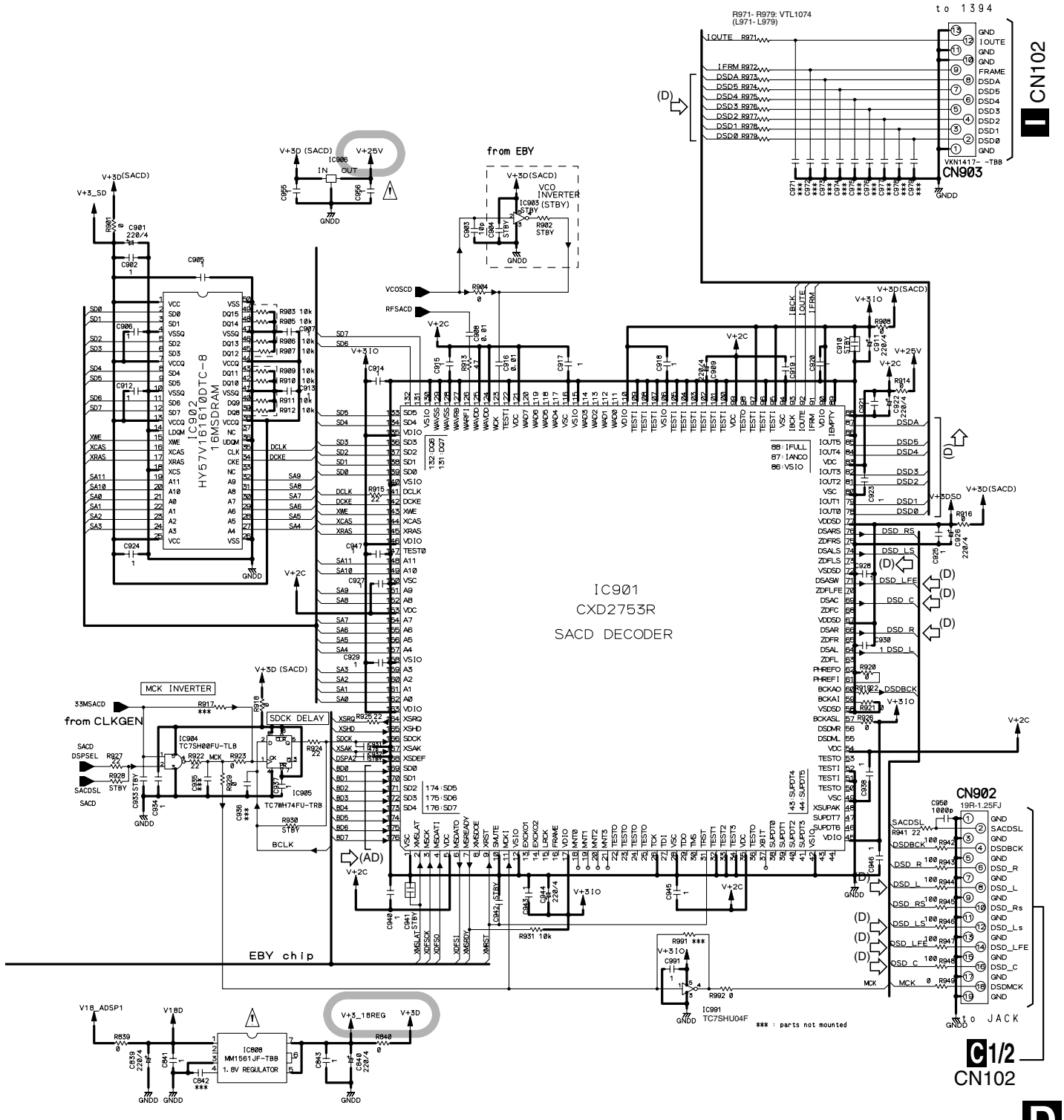


: The power supply is shown with the marked box.

(AD) : AUDIO DATA SIGNAL ROUTE

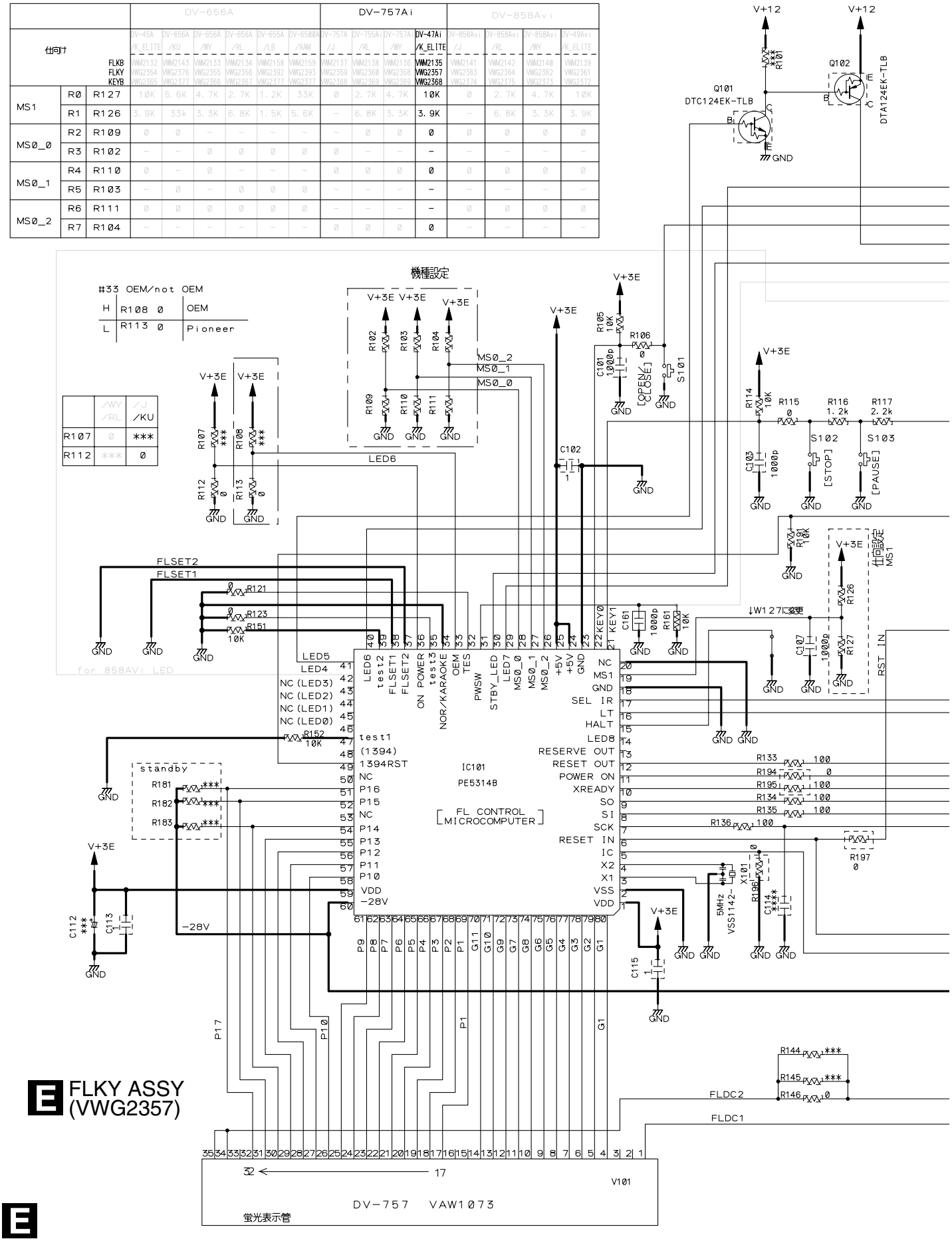
(D) : AUDIO (DIGITAL) SIGNAL ROUTE

Note
1608
1608



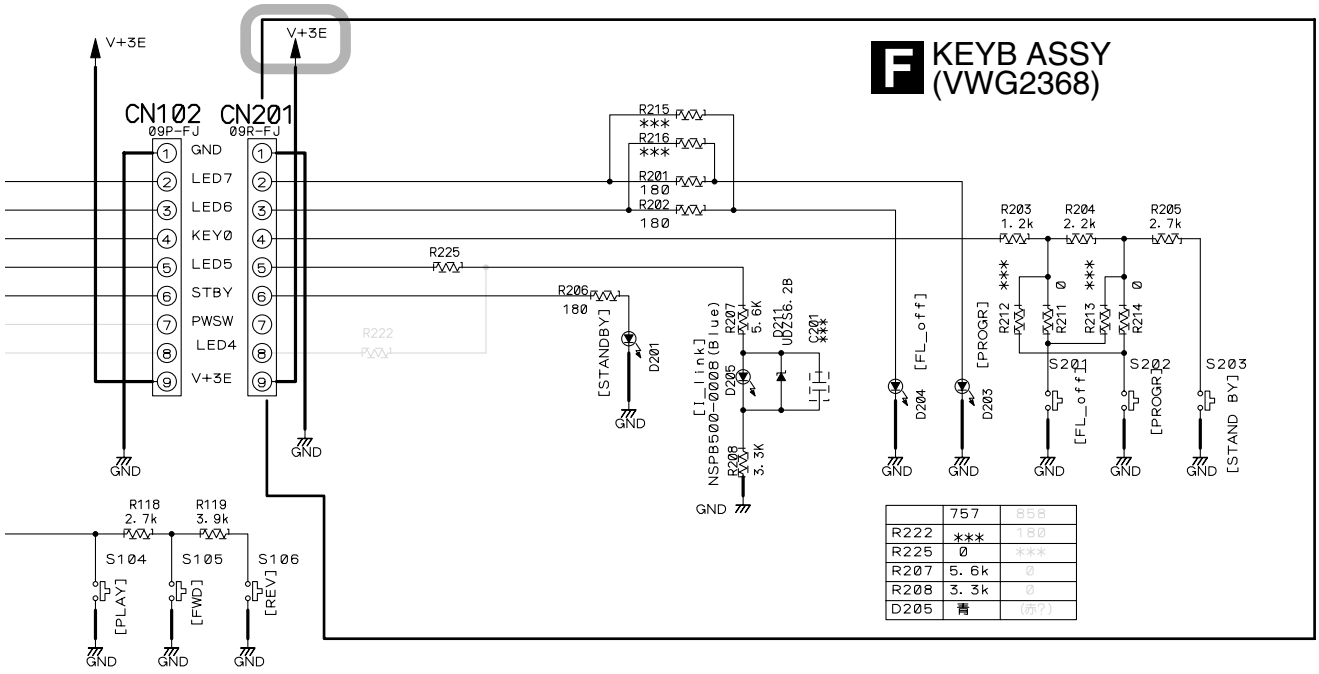
3.10 FLKY and KEYB ASSYS

			DV-656A						DV-757Ai				DV-858Avi			
仕向け			DV-45A /K_ELITE	DV-656A /KU	DV-656A /MY	DV-656A /RL	DV-655A /LB	DV-6500A /RAM	DV-757A /J	DV-755Ai /RL	DV-757A /MY	DV-47Ai /K_ELITE	DV-858Avi /J	DV-858Avi /RL	DV-858Avi /MY	DV-49Avi /K_ELITE
		FLKB	VWM2132	VWM2143	VWM2133	VWM2134	VWM2158	VWM2159	VWM2137	VWM2138	VWM2136	VWM2135	VWM2141	VWM2142	VWM2140	VWM2139
		FLKY	VWG2354	VWG2376	VWG2355	VWG2356	VWG2392	VWG2393	VWG2359	VWG2360	VWG2358	VWG2357	VWG2363	VWG2364	VWG2362	VWG2361
		KEYB	VWG2365	VWG2377	VWG2366	VWG2367	VWG2377	VWG2377	VWG2368	VWG2369	VWG2369	VWG2368	VWG2374	VWG2375	VWG2373	VWG2372
MS1	R0	R127	10K	5.6K	4.7K	2.7K	1.2K	33K	0	2.7K	4.7K	10K	0	2.7K	4.7K	10K
	R1	R126	3.9K	33k	3.3K	6.8K	1.5K	5.6K	–	6.8K	3.3K	3.9K	–	6.8K	3.3K	3.9K
MS0_0	R2	R109	0	0	–	–	–	–	–	0	0	0	0	0	0	0
	R3	R102	–	–	0	0	0	0	0	–	–	–	–	–	–	–
MS0_1	R4	R110	0	–	0	–	–	–	0	0	0	0	0	0	0	0
	R5	R103	–	0	–	0	0	0	–	–	–	–	–	–	–	–
MS0_2	R6	R111	0	0	0	0	0	0	–	–	–	–	0	0	0	0
	R7	R104	–	–	–	–	–	–	0	0	0	0	–	–	–	–

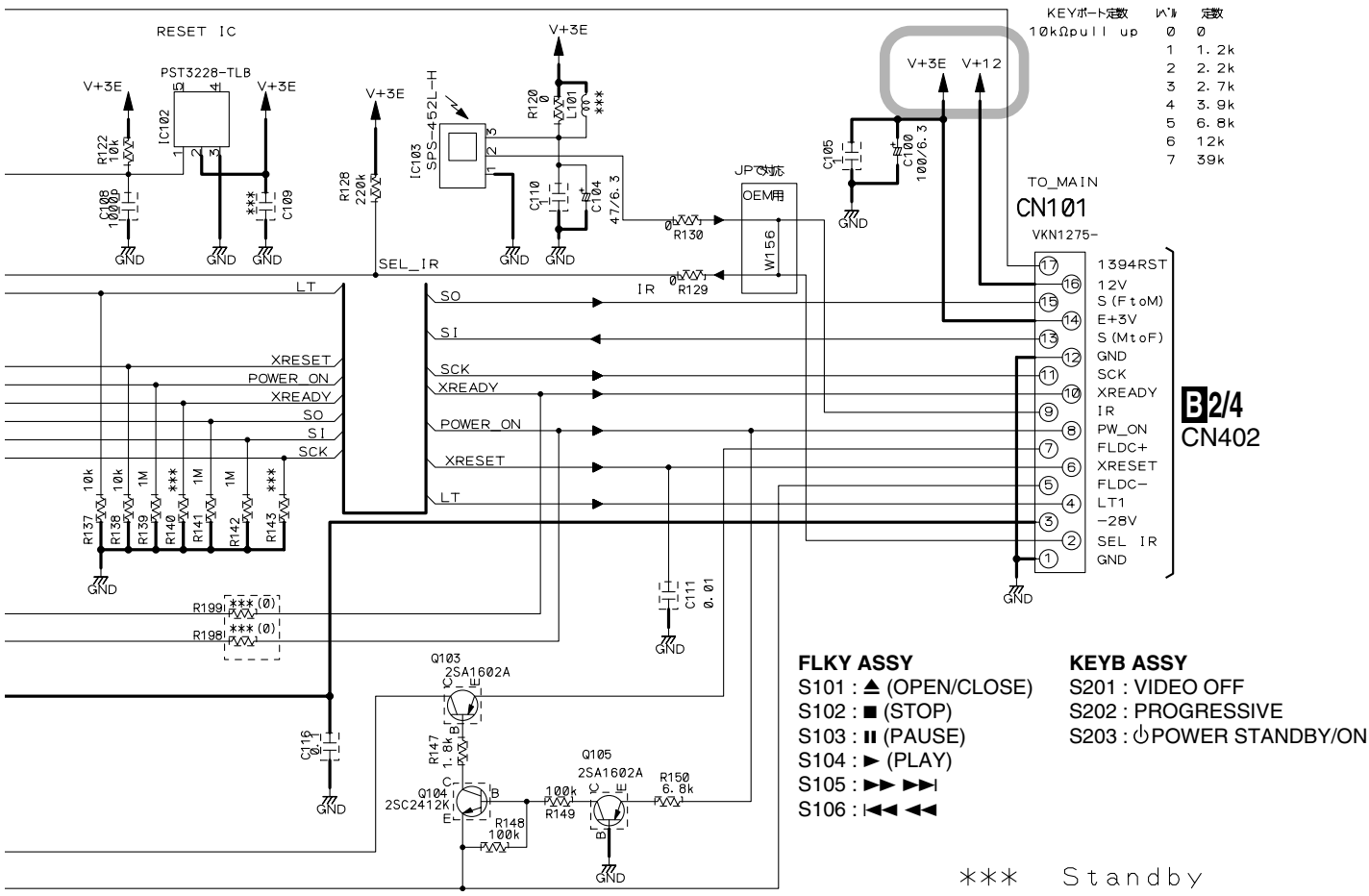


E FLKY ASSY (VWG2357)

: The power supply is shown with the marked box.



	757	858
R222	***	180
R225	0	***
R207	5.6k	0
R208	3.3k	0
D205	青	(赤?)



KEYボード定数 10kΩpull up

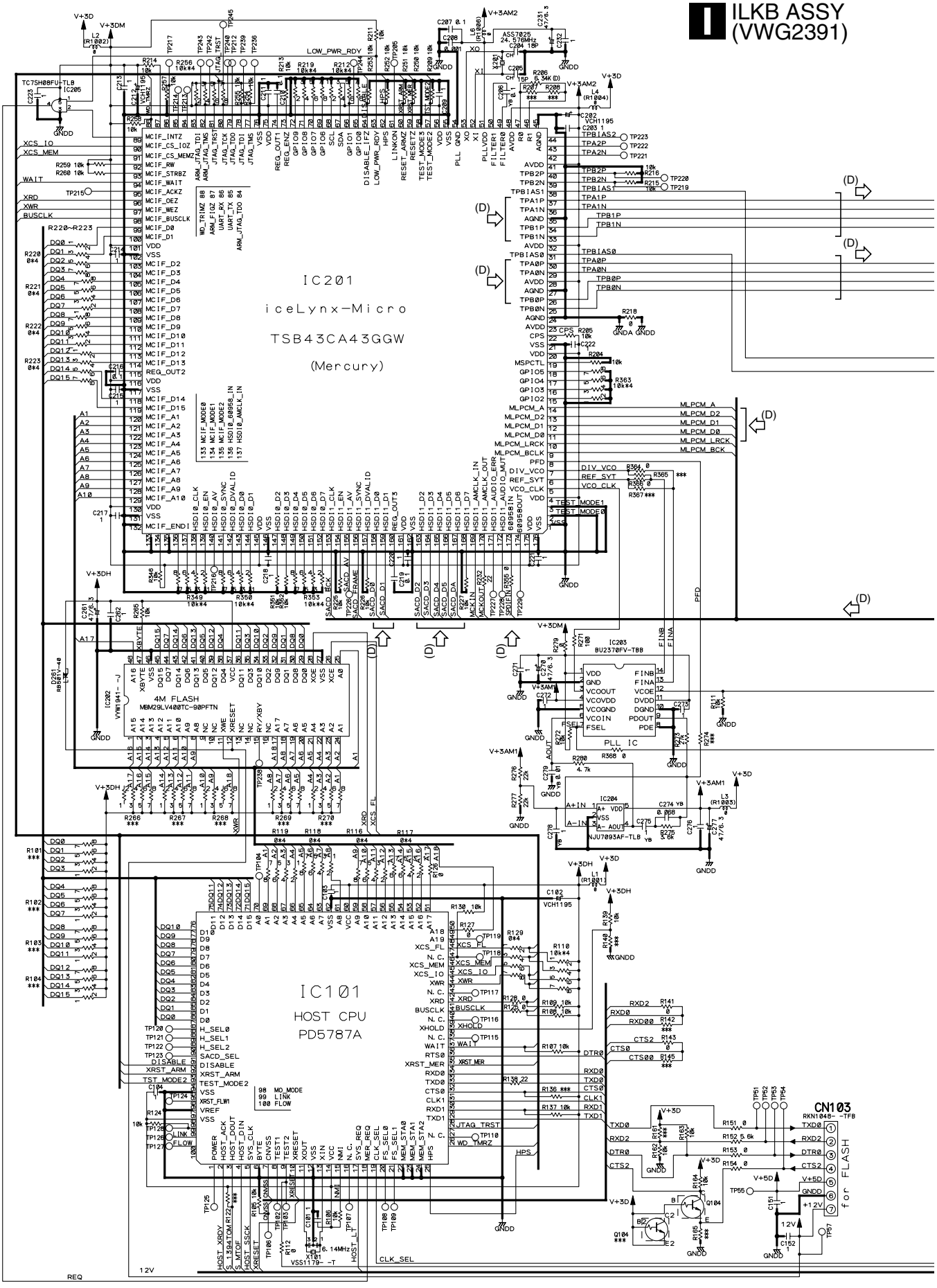
ﾚﾍﾞﾙ	定数
0	0
1	1. 2k
2	2. 2k
3	2. 7k
4	3. 9k
5	6. 8k
6	12k
7	39k

FLKY ASSY
S101 : ▲ (OPEN/CLOSE)
S102 : ■ (STOP)
S103 : ❚❚ (PAUSE)
S104 : ► (PLAY)
S105 : ►► ►❙
S106 : ❙◄◄ ◄◄

KEYB ASSY
S201 : VIDEO OFF
S202 : PROGRESSIVE
S203 : ⏻POWER STANDBY/ON

*** Standby

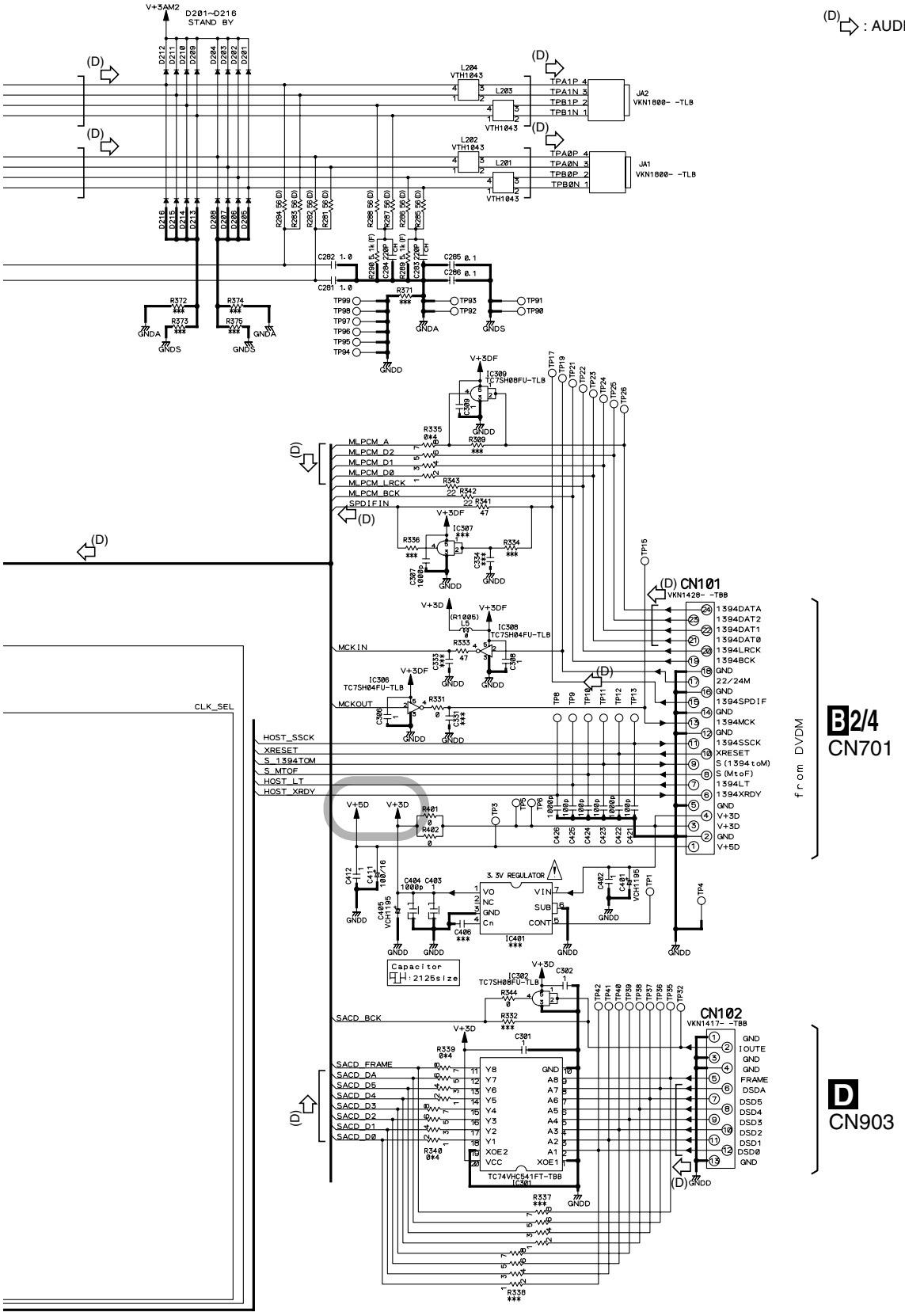
3.11 ILKB ASSY



All *** are stand by.

: The power supply is shown with the marked box.

(D) : AUDIO (DIGITAL) SIGNAL ROUTE

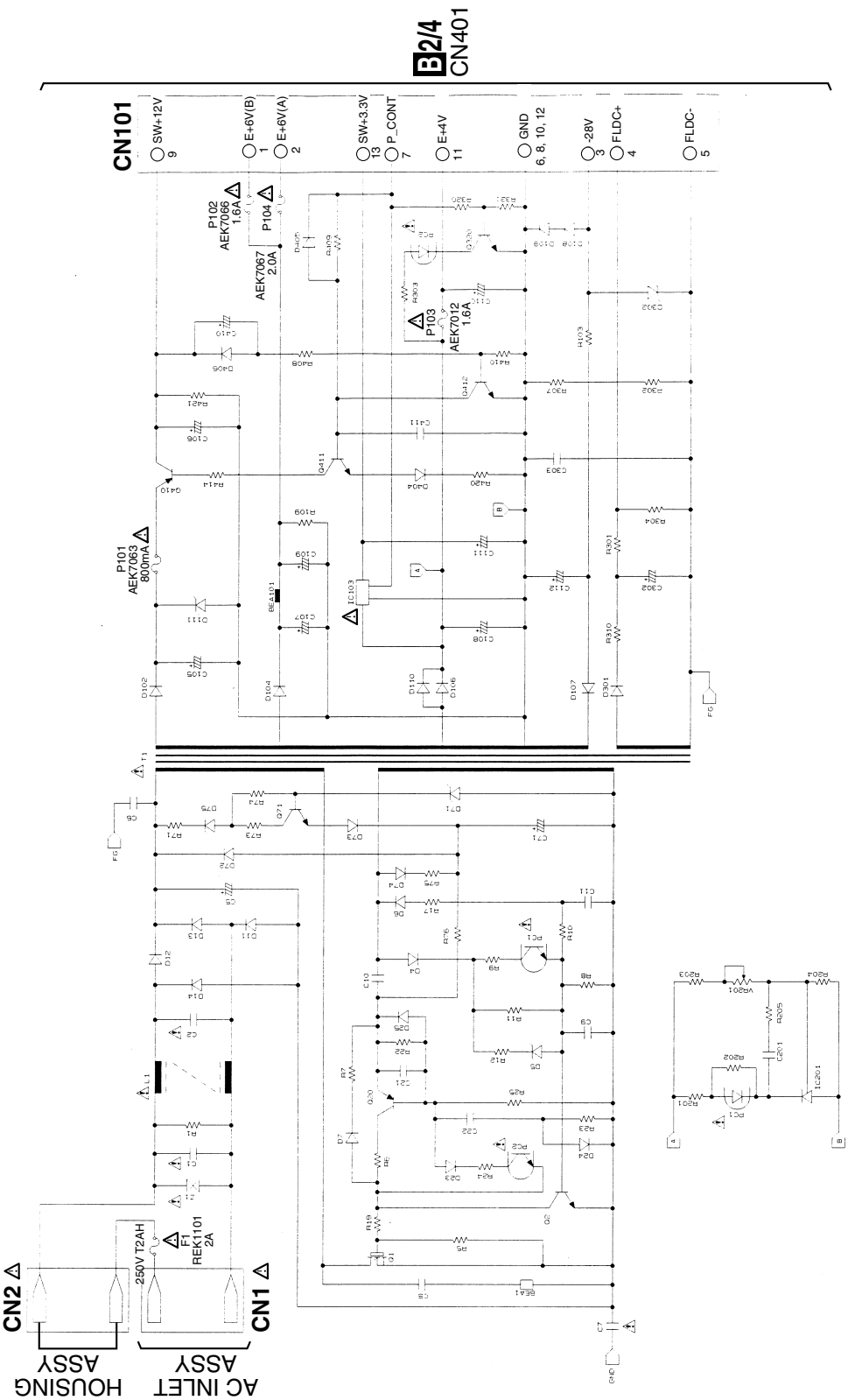


3.12 POWER SUPPLY UNIT

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. 491.800 MFD, BY LITTELFUSE INC. FOR P101 (AEK7063).

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. 49101.6 MFD, BY LITTELFUSE INC. FOR P102 (AEK7066).

CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. 491002 MFD, BY LITTELFUSE INC. FOR P104 (AEK7067).



CAUTION : FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE ONLY WITH SAME TYPE NO. 49101.6 MFD, BY LITTELFUSE INC. FOR P103 (AEK7012).

• NOTE FOR FUSE REPLACEMENT

CAUTION - FOR CONTINUED PROTECTION AGAINST RISK OF FIRE. REPLACE WITH SAME TYPE AND RATINGS ONLY.

G POWER SUPPLY UNIT (VWR1361)

≪ NOTE OF SPARE PARTS IN POWER SUPPLY (SYPS) UNIT ≫

- In case of repairing, use the described parts only to prevent an accident.
- Please write the red ✓ mark on the board when the primary section of POWER SUPPLY (SYPS) Unit is repaired.
- Please take care to keep the space, not touching other parts when replacing the parts.

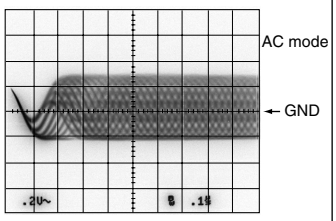
3.13 WAVEFORMS [DVDM ASSY]

Note : The encircled numbers denote measuring point in the schematic diagram.

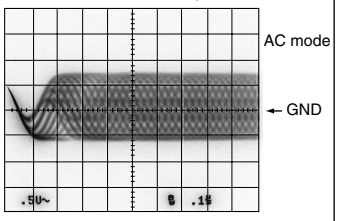
B DVDM ASSY

Measurement condition : No. 1 to 4 and 6 to 11 : MJK1, Title 1-chp 1
No. 5 : CD, ABEX-784 Track 1
No. 12 to 14 : DVD-REF-A1, T2-Chap.1
No. 15 to 20 : DVD-REF-A1, T2-Chap.19

1 **IC101-pin 3 (RF)**
V: 200mV/div. H: 0.1µsec/div.

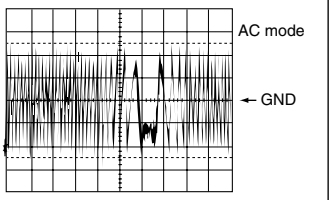


2 **Q106-emitter (RFO)**
V: 500mV/div. H: 0.1µsec/div.

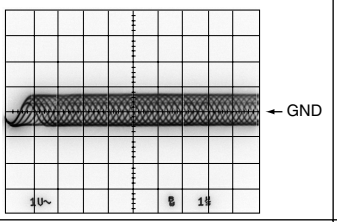


3

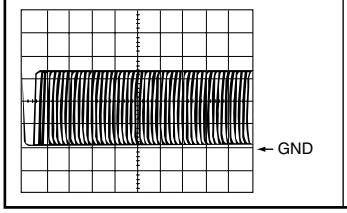
4 **IC101-pin 42 (Tracking Error)**
(AI-Inner Tracking Off)
V: 500mV/div. H: 2msec/div.



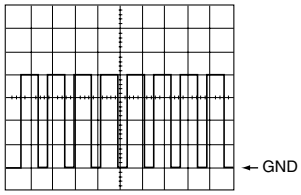
5 **IC201 - pin 39 (EFM before slice)**
V: 0.5V/div. H: 0.2µsec/div.



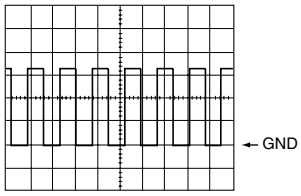
6 **IC201 - pin 1 (EFM)**
V: 1V/div. H: 0.2µsec/div.



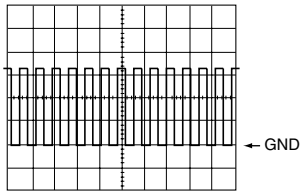
7 **IC251 - pin 24 (FG)**
V: 1V/div. H: 5msec/div.



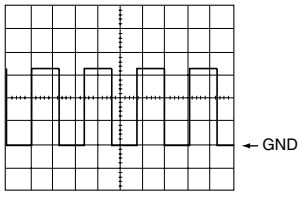
8 **Foot of R261 (FPWM)**
V: 1V/div. H: 10µsec/div.



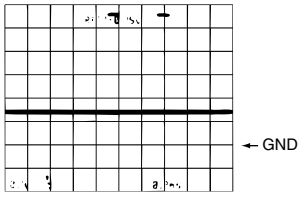
9 **Foot of R262 (VPWM)**
V: 1V/div. H: 10µsec/div.



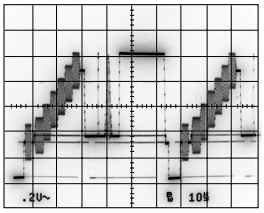
10 **Foot of R263 (PPWM)**
V: 1V/div. H: 0.2msec/div.



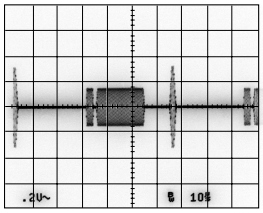
11 **Foot of R264 (RPWM)**
V: 1V/div. H: 5msec/div.



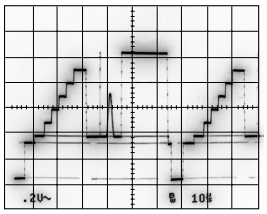
12 **Foot of R964 (V)**
V: 0.2V/div. H: 10µsec/div.



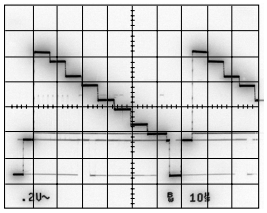
13 **Foot of R963 (C)**
V: 0.2V/div. H: 10µsec/div.



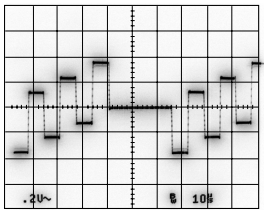
14 **Foot of R960 (Y)**
V: 0.2V/div. H: 10µsec/div.



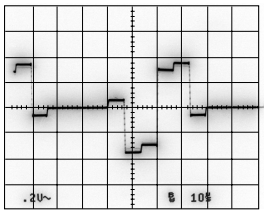
15 **Foot of R959 (Y)**
V: 0.2V/div. H: 10µsec/div.



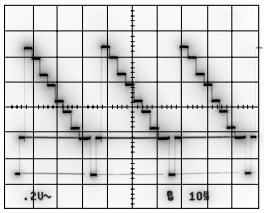
16 **Foot of R958 (Pb)**
V: 0.2V/div. H: 10µsec/div.



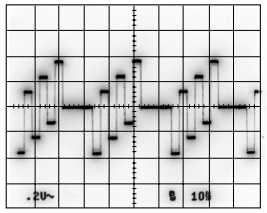
17 **Foot of R957 (Pr)**
V: 0.2V/div. H: 10µsec/div.



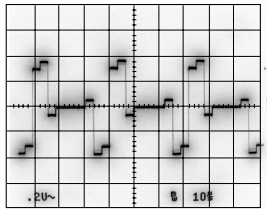
18 **Foot of R959 (Y)**
V: 0.2V/div. H: 10µsec/div.



19 **Foot of R958 (Pb)**
V: 0.2V/div. H: 10µsec/div.



20 **Foot of R957 (Pr)**
V: 0.2V/div. H: 10µsec/div.



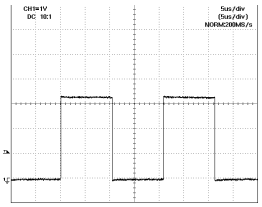
3.14 WAVEFORMS [JACB ASSY]

Note : The encircled numbers denote measuring point in the schematic diagram.

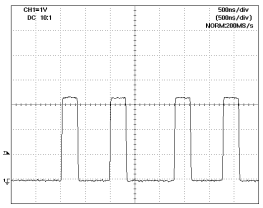
C JACB ASSY

Measurement condition : No. 21 to 25 : DVD-REF-A1, T2-Chap.1

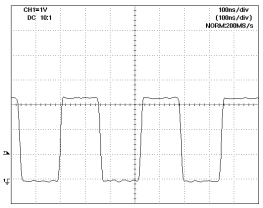
21 **IC301-pin 4 (LRCK)**
V: 1V/div. H: 5µsec/div.



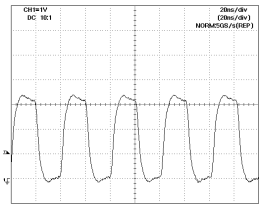
22 **IC301-pin 5 (DATA0)**
V: 1V/div. H: 500nsec/div.



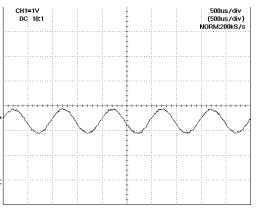
23 **IC301-pin 6 (BCK)**
V: 1V/div. H: 100nsec/div.



24 **IC301-pin 7 (PMCK)**
V: 1V/div. H: 20nsec/div.



25 **IC302 - pin 1 (Analog OUT)**
V: 1V/div. H: 500µsec/div.



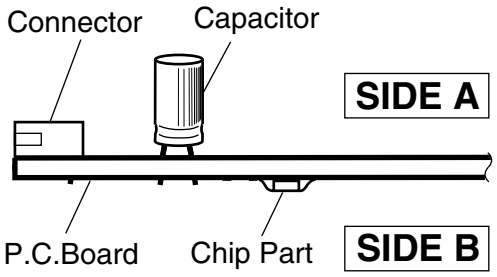
4. PCB CONNECTION DIAGRAM
4.1 LOAB ASSY

NOTE FOR PCB DIAGRAMS :

1. Part numbers in PCB diagrams match those in the schematic diagrams.
2. A comparison between the main parts of PCB and schematic diagrams is shown below.

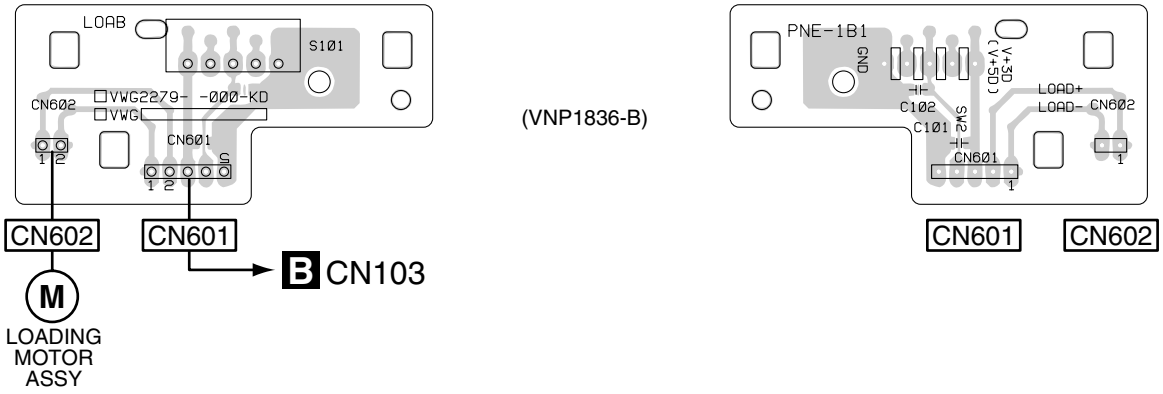
Symbol In PCB Diagrams	Symbol In Schematic Diagrams	Part Name
B C E	B C E B C E	Transistor
B C E	B C E B C E	Transistor with resistor
D G S	D G S D G S	Field effect transistor
		Resistor array
		3-terminal regulator

3. The parts mounted on this PCB include all necessary parts for several destinations.
   For further information for respective destinations, be sure to check with the schematic diagram.
4. View point of PCB diagrams.



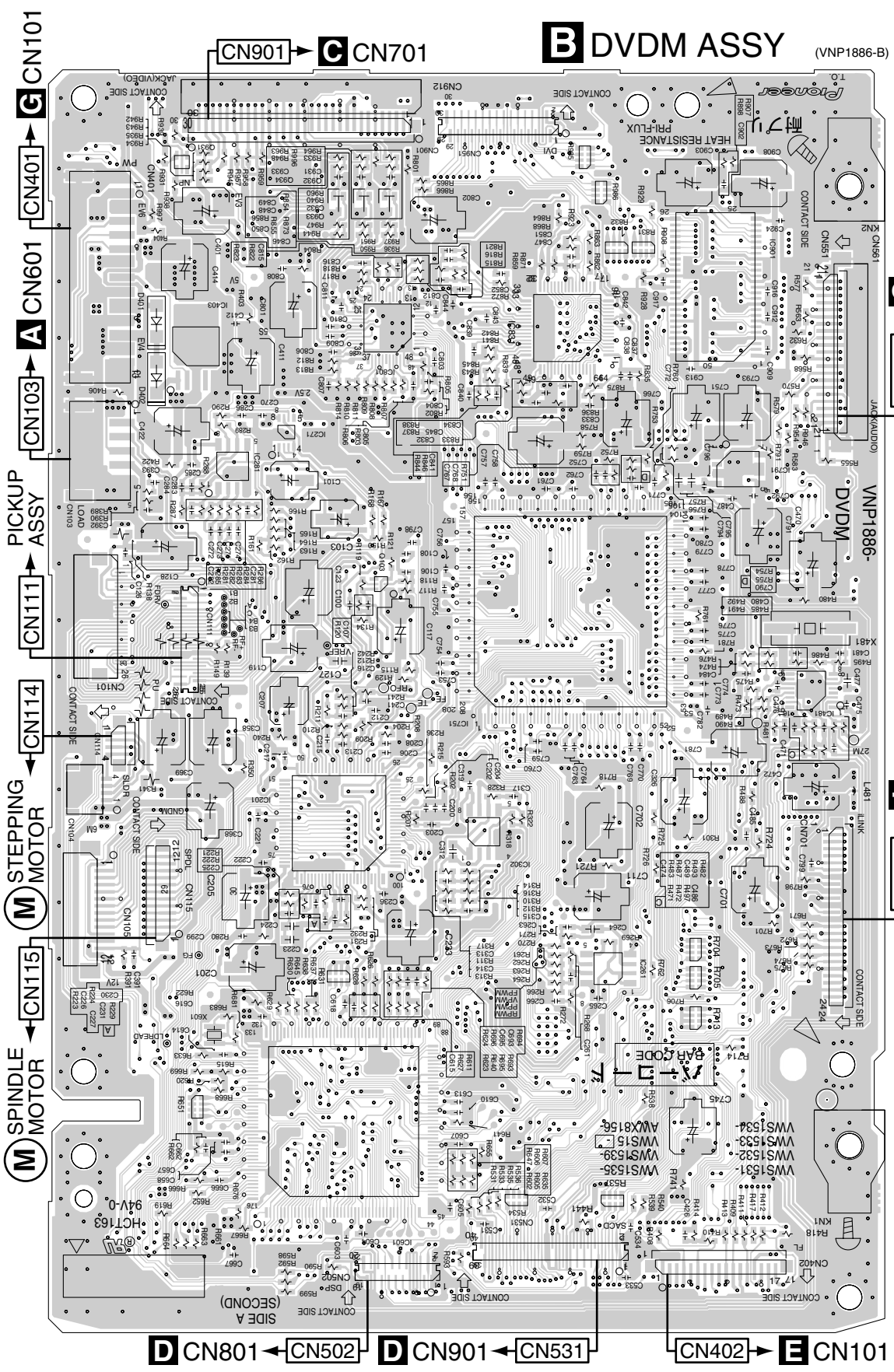
SIDE A **SIDE B**

A LOAB ASSY



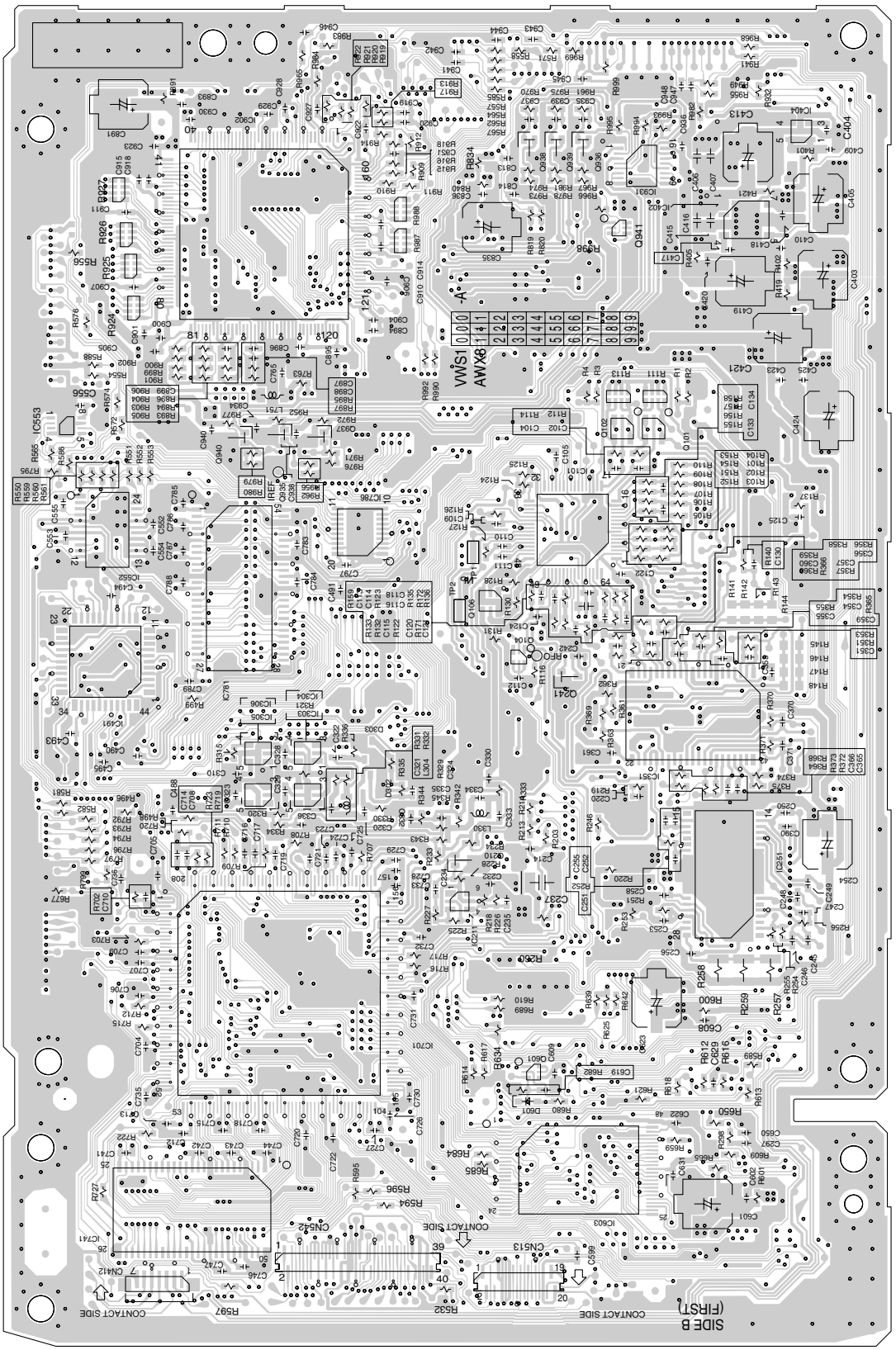
4.2 DVDM ASSY

SIDE A



SIDE B

B DVDM ASSY (VNP1886-B)

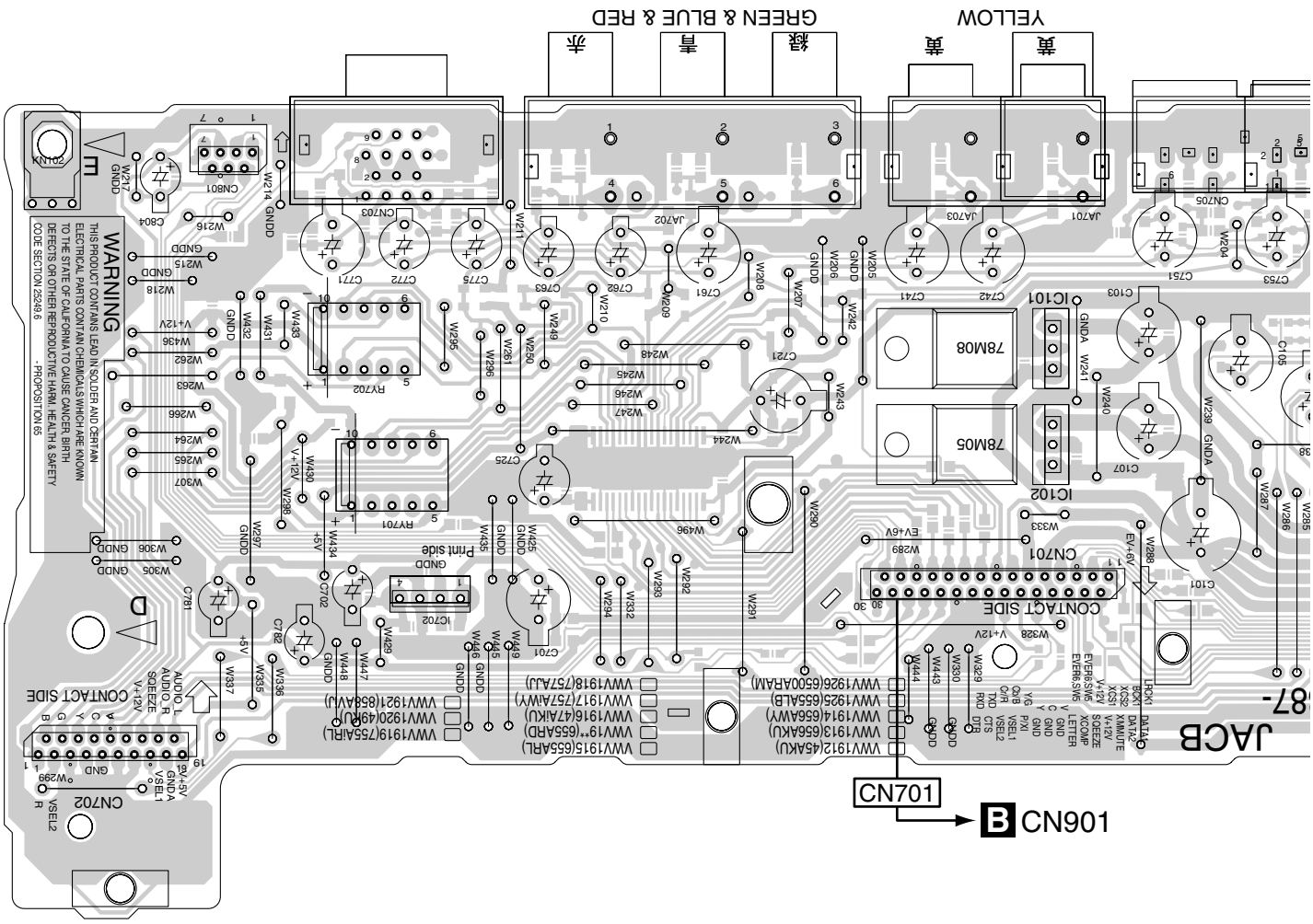


IC404
IC902
Q938
Q939
Q936
IC931
IC402
Q941
Q937
Q102
IC553
Q940 Q101
IC101
Q935
IC786
IC552
Q106
Q104
Q241
IC304
IC781
IC491
IC351
Q210
IC251
IC211
IC701
Q601
IC603
IC741

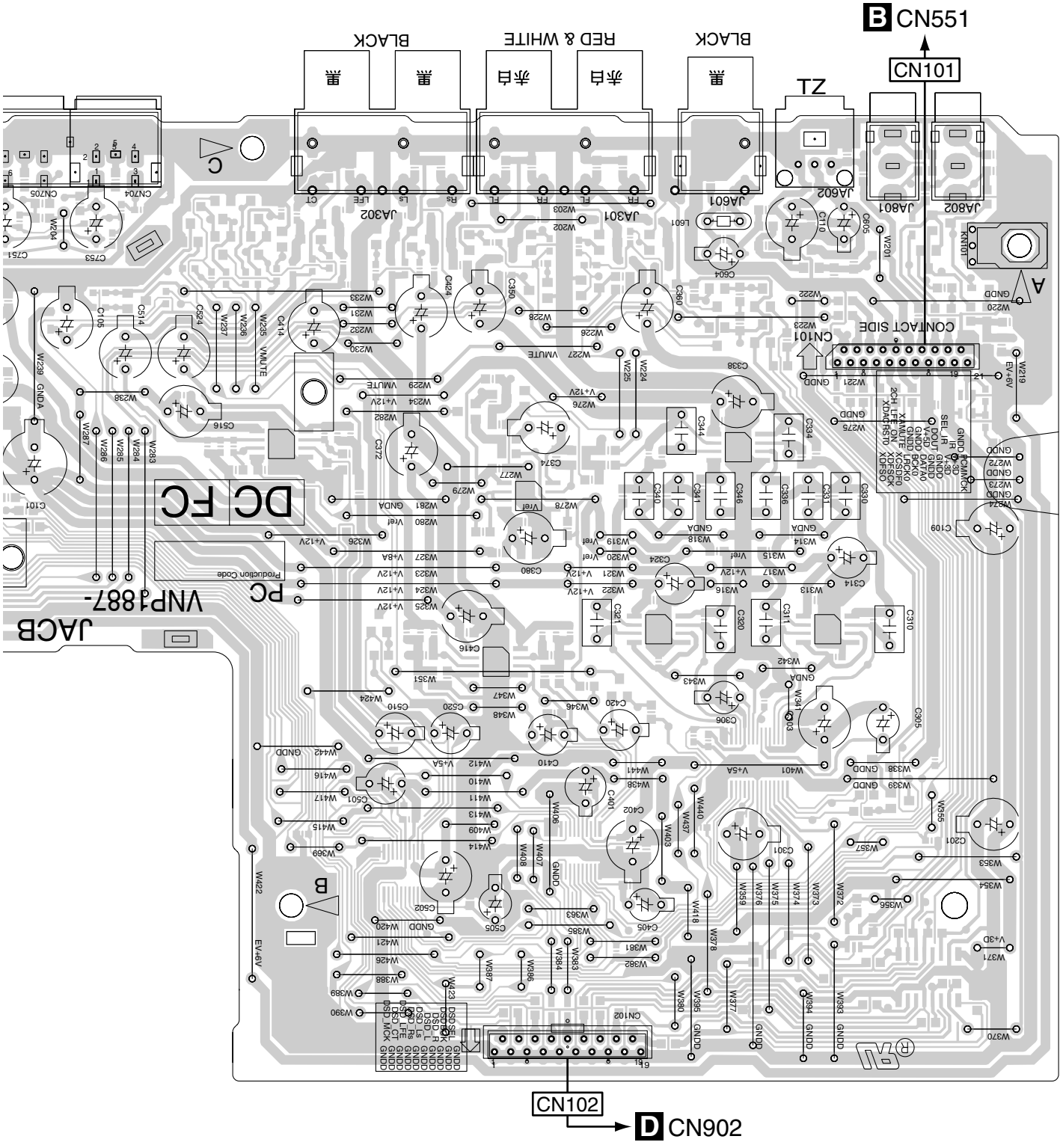
4.3 JACB ASSY

SIDE A

C JACB ASSY (VNP1887-C)



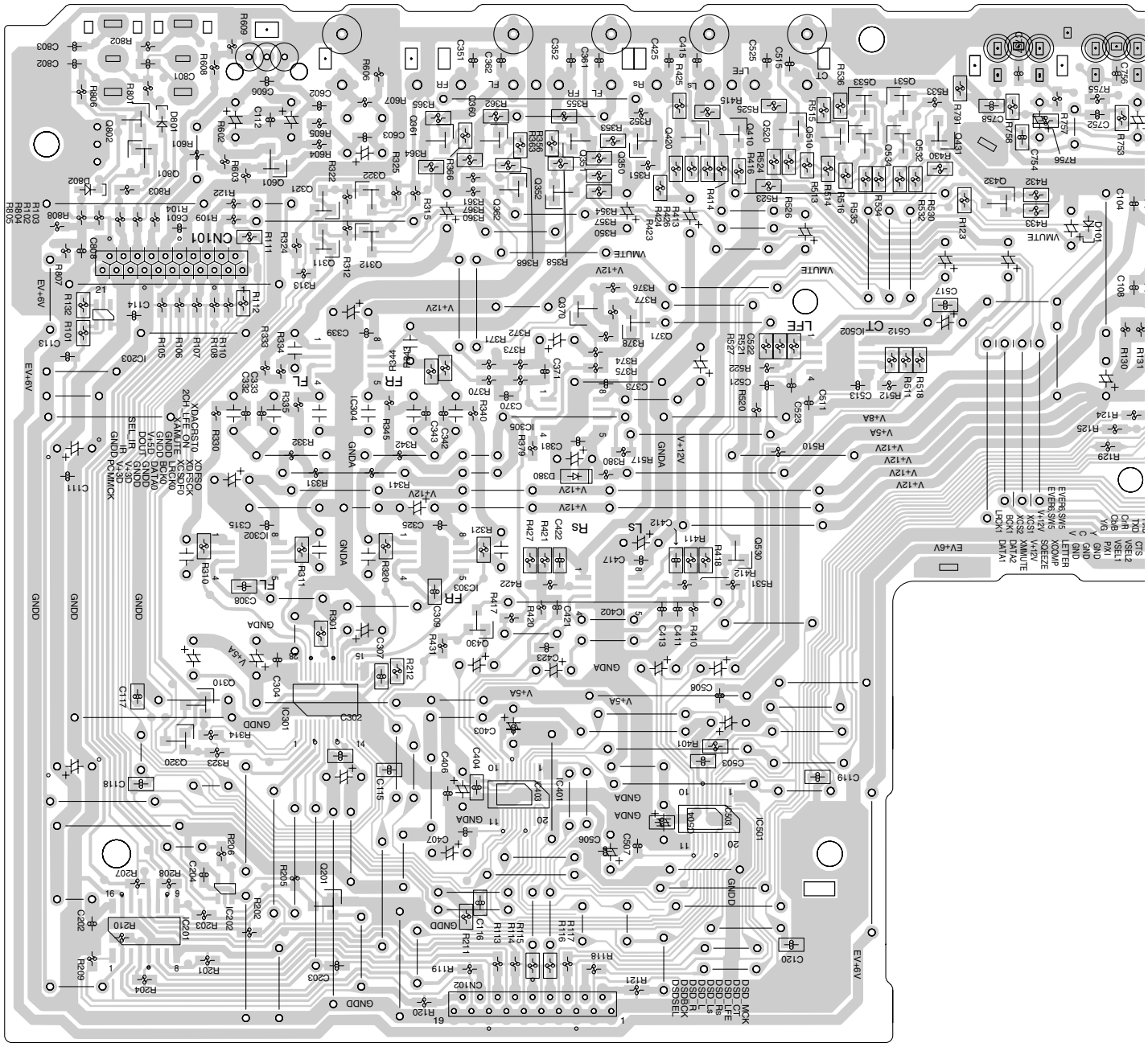
SIDE A


B CN551
CN101
ZL
BLACK
RED & WHITE
BLACK
黒
黒
黒
赤白
赤白
JA801
JA802
JA602
JA601
JA301
JA302
CONTACT SIDE
CN101
A
C
B
DC FC
PC
Production Code
VNP4887-
JACB
CN102
D CN902

SIDE B

C JACB ASSY (VNP1887-C)

CN101



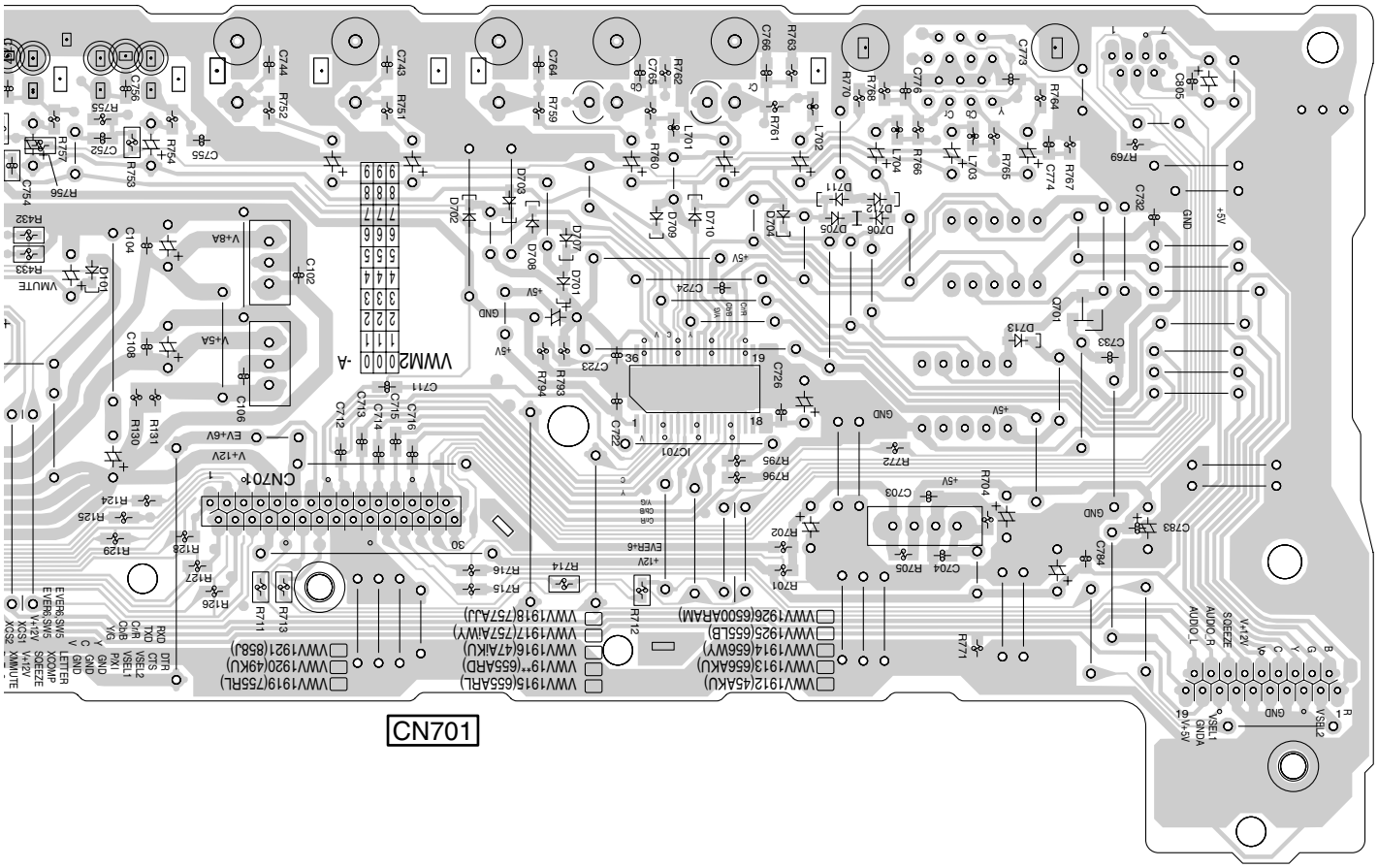
CN102

Q802 Q801 Q601 Q322 Q361 Q360 Q352 Q351 Q350 Q420 Q520 Q510 Q533 Q531 Q431 Q432
Q320 Q310 Q321 Q362 Q370 Q371 Q410 Q532
Q311 Q312 Q430 Q530 Q534
Q201

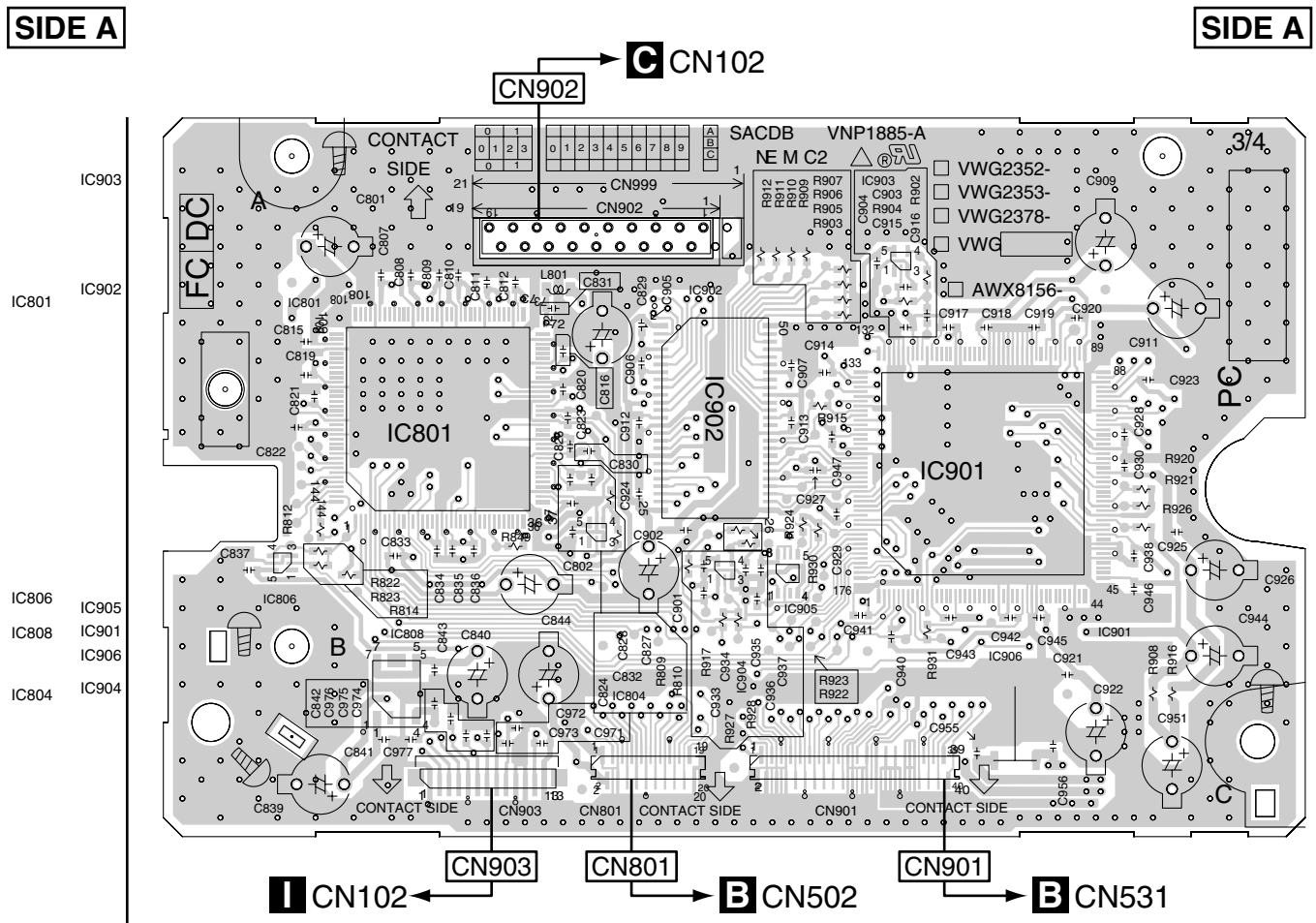
IC302 IC304 IC305 IC402 IC503
IC202 IC301 IC303 IC403 IC501
IC201 IC401

C

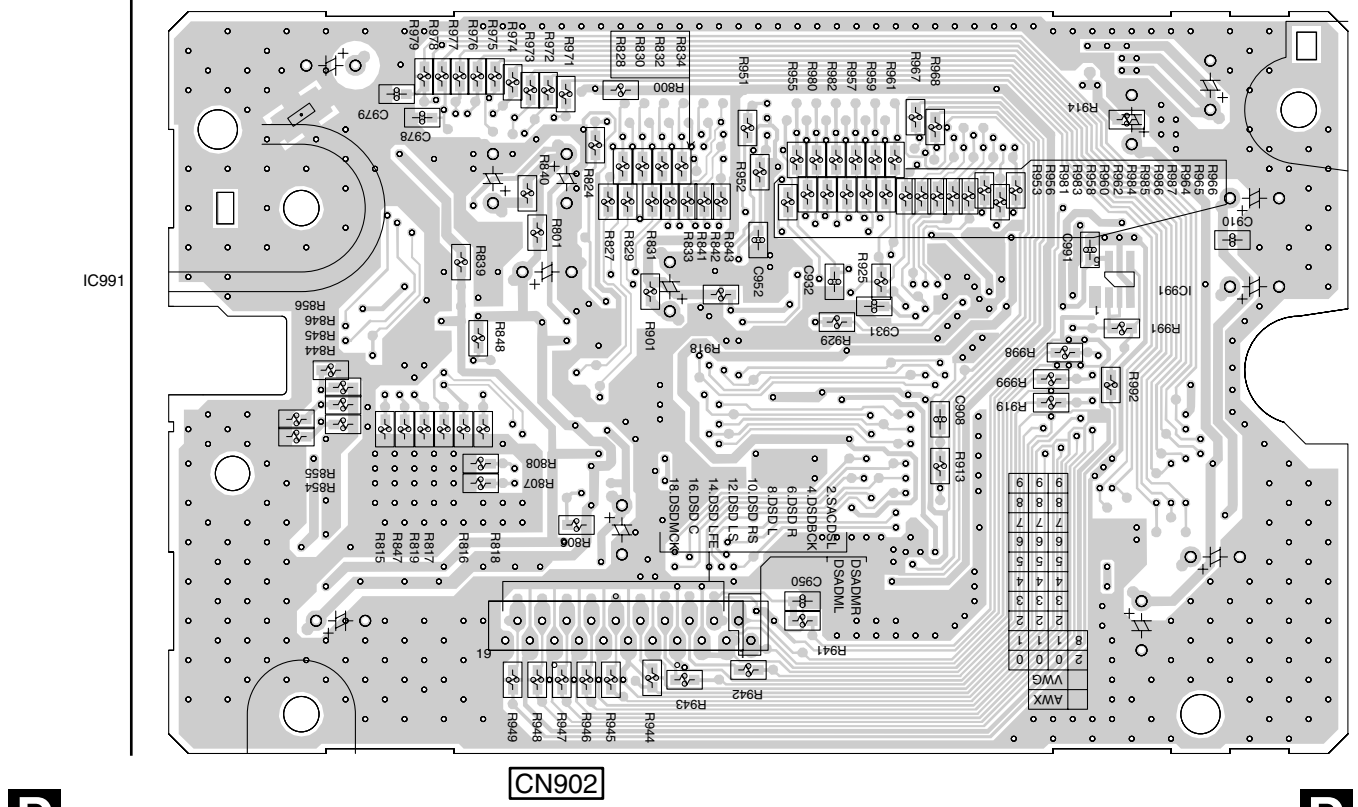
SIDE B


CN701
Q701
IC701
VWM2-A
CN707
VWV1912(45AKU)
VWV1913(656AKU)
VWV1914(656WY)
VWV1925(655LB)
VWV1926(6500ARAM)
VWV1915(655ARL)
VWV19**(655ARD)
VWV1916(47AIKU)
VWV1917(757AIWY)
VWV1918(757AJJ)
VWV1920(49KU)
VWV1921(858J)
VWV1919(758RL)
V+8A
V+5A
V+12V
EV+6V
+5V
+12V
GND
EVER6.SW5
EVER6.SW5
V+12V
XGS1
XGS2
XMMUTE
LETTER
XCOMP
SQEEZE
V+12V
GND
GND
GND
PXI1
PXI0
VSEL1
CHR
CHB
VSEL2
CTS
DTR
RXD
AUDIO_R
AUDIO_L
SQEEZE
V+12V
GNDA
VSEL1
19V-5V
VSEL2

4.4 SACDB ASSY



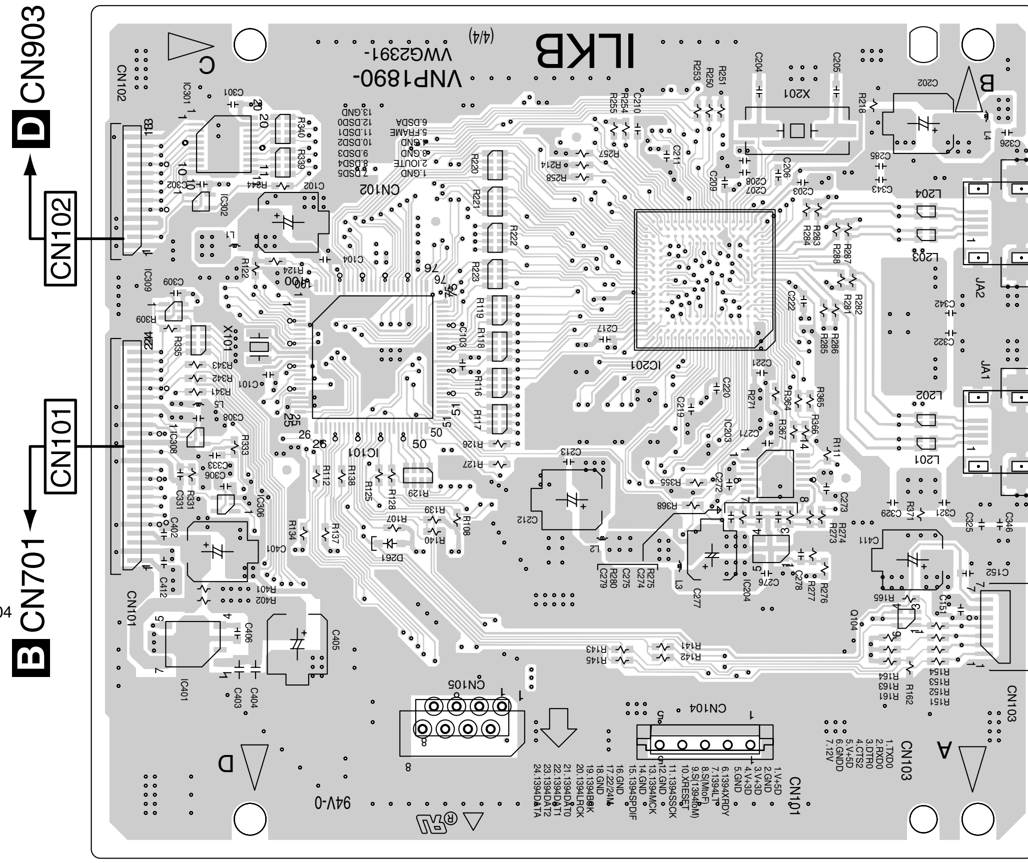
D SACDB ASSY (VNP1885-A)



4.5 ILKB ASSY

SIDE A **SIDE A**

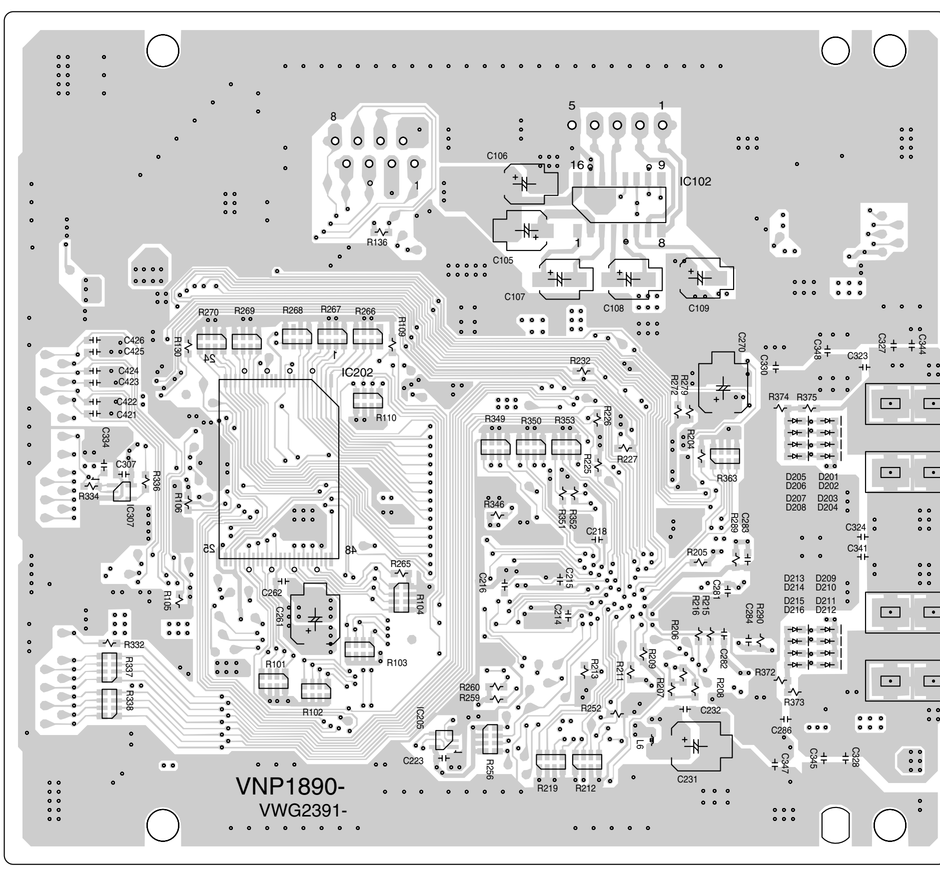
IC301
IC302
IC309
IC201
IC308 IC203
IC101
IC306
IC204
Q104
IC401



I ILKB ASSY (VNP1890-A)

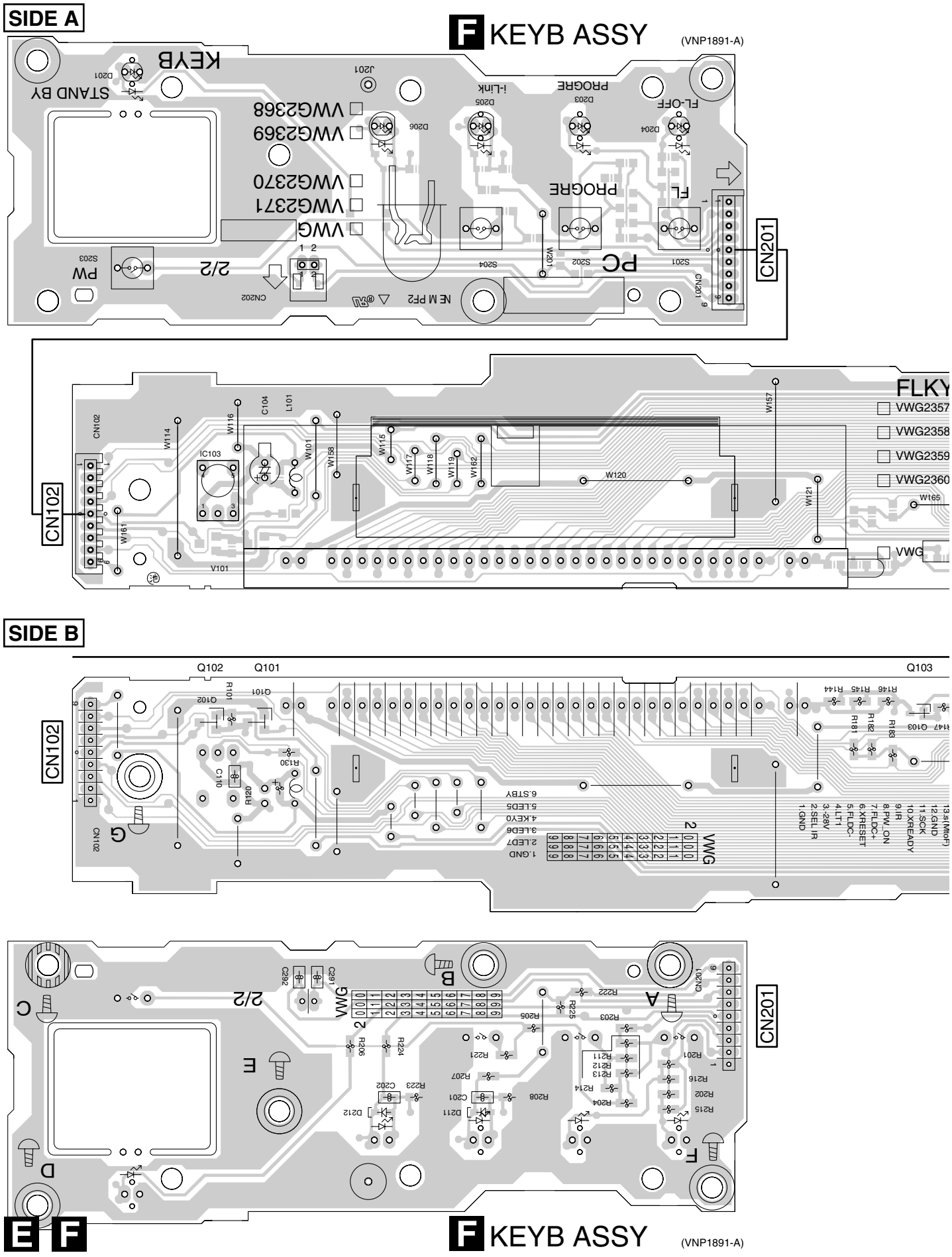
SIDE B **SIDE B**

IC102
IC202
IC307
IC205



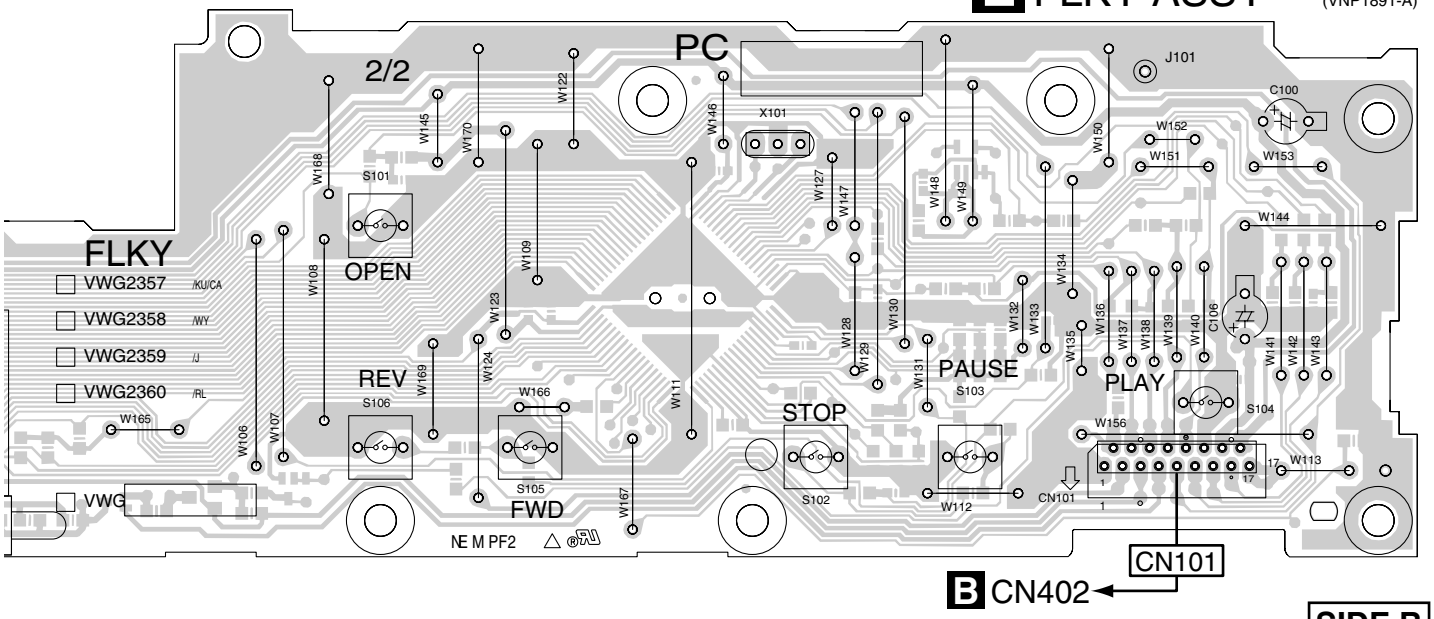
I I

4.6 FLKY and KEYB ASSYS

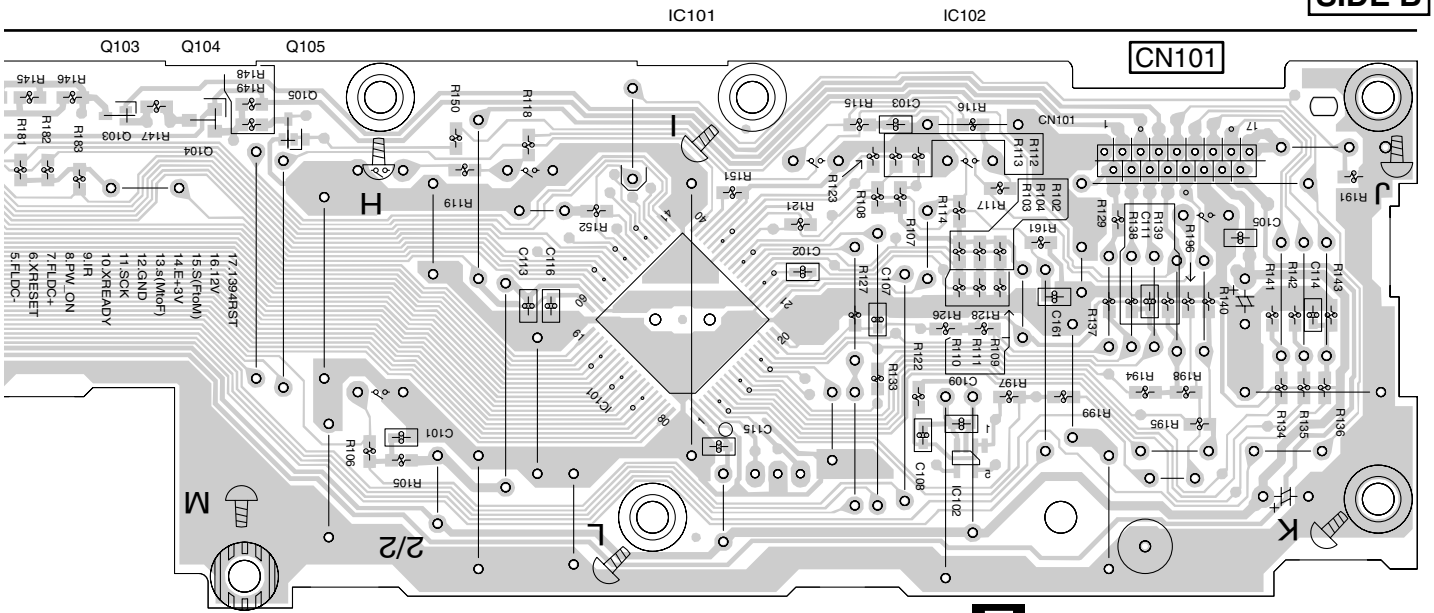


SIDE A

E FLKY ASSY (VNP1891-A)

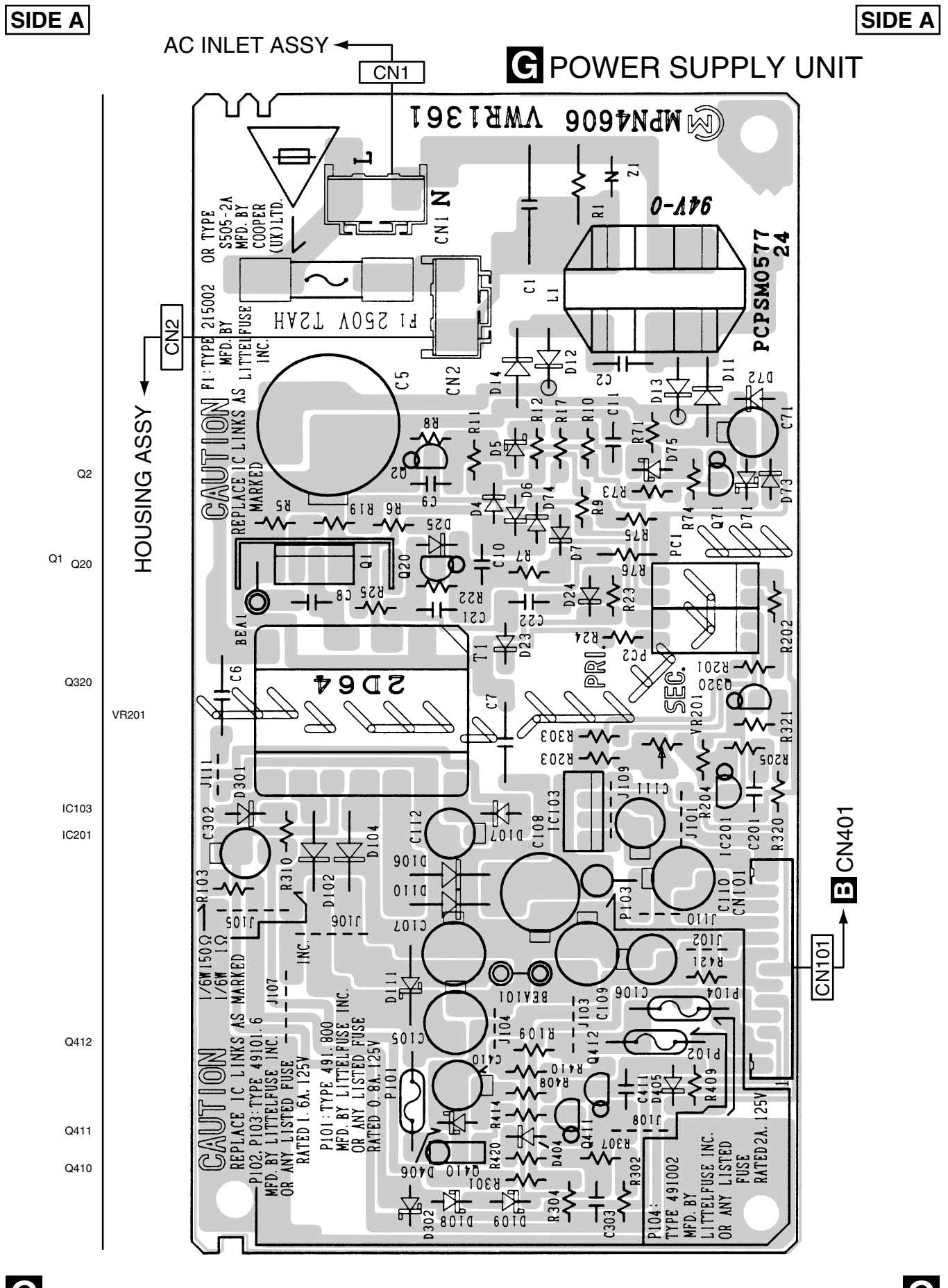


SIDE B



E FLKY ASSY (VNP1891-A)

4.7 POWER SUPPLY UNIT



5. PCB PARTS LIST

NOTES: ● *Parts marked by "NSP" are generally unavailable because they are not in our Master Spare Parts List.*
● *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
● *When ordering resistors, first convert resistance values into code form as shown in the following examples.*
Ex.1 When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J=5%, and K=10%).

560 Ω	→	*56 x 10¹* →	*561*	*RD1/4PU 5 6 1 J*
47k Ω	→	*47 x 10³* →	*473*	*RD1/4PU 4 7 3 J*
0.5 Ω	→	*R50*		*RN2H R 5 0 K*
1 Ω	→	*1R0*		*RS1P 1 R 0 K*

Ex.2 When there are 3 effective digits (such as in high precision metal film resistors).

5.62k Ω	→	*562 x 10¹* →	*5621*	*RN1/4PC 5 6 2 1 F*

LIST OF ASSEMBLIES

Mark	No.	Description	Part No.
NSP	1	LOADING MECHANISM ASSY	VWT1203
NSP	2	LOAB ASSY	VWG2346
	1	DVDM ASSY	VWS1534
	1	JCSB ASSY	VWM2148
	2	JACB ASSY	VWV1916
	1	SACDB ASSY	VWG2353
	1	FLKB ASSY	VWM2135
	2	FLKY ASSY	VWG2357
	2	KEYB ASSY	VWG2368
	1	ILKB ASSY	VWG2391
⚠	1	POWER SUPPLY UNIT	VWR1361

A LOAB ASSY

SWITCHES AND RELAYS

Mark	No.	Description	Part No.
	S101	REAF SWITCH	VSK1011

OTHERS

Mark	No.	Description	Part No.
	CN602	CONNCTOR	S2B-PH-K
	CN601	CONNCTOR	S5B-PH-K
		PRINTED CIRCUIT BOARD	VNP1836

B DVDM ASSY

SEMICONDUCTORS

Mark	No.	Description	Part No.
	IC831		ADV7300AKST
	IC261, IC302		BA4510F
	IC251		BA6664FM
	IC741, IC901		HY57V161610DTC-8
	IC101		LA9704W
	IC201		LC78652W
	IC781		M2V64S40DTP-7
	IC351		M56788AFP
	IC751		M65776AFP
⚠	IC404		MM1385EN
⚠	IC791		MM1561JF
⚠	IC402		MM1565AF
	IC552		PD0274A
	IC601		PD6345A
	IC701		PE5286A
	IC491		PE9015A
	IC902		PM0033A
⚠	IC403		PQ025EZ01ZP
	IC481		SM8707HV
	IC786		TC74VHC541FT
	IC303, IC304, IC306		TC7SZU04F
	IC553		TC7WH157FU
	IC211		TK15404M
	IC603		VYW2025
	Q210, Q932–Q934, Q936		2SA1576A
	Q938, Q939		2SA1576A
	Q241		DTC114EUA
	Q101, Q102, Q106		HN1A01F
	Q103, Q104		HN1B04FU
	Q931		RN1911
	Q601, Q941		RN4982
	D302, D303		KV1470
	D401, D402		RB051L-40
	D601		RB501V-40

COILS AND FILTERS

Mark	No.	Description	Part No.
	L304		LCYA1R2J2520
	L4080, L4090, L4100	CHIP BEADS	VTL1074
	L4110, L4120	CHIP BEADS	VTL1074
	L4130, L4820, L4880	CHIP BEADS	VTL1074
	L4910, L4930	CHIP BEADS	VTL1074
	L652	CHIP BEADS	VTL1074
	L4720	CHIP BEADS	VTL1079
	L4710	CHIP BEADS	VTL1081
	L4800, L481	CHIP BEADS	VTL1084

CAPACITORS

Mark	No.	Description	Part No.
	C480, C481, C662		CCSRCH100D50
	C121, C532, C6270, C950		CCSRCH101J50
	C953–C955		CCSRCH101J50
	C314, C474, C798		CCSRCH150J50
	C100, C133		CCSRCH151J50
	C120		CCSRCH181J50
	C484, C485, C487, C667		CCSRCH220J50
	C134, C324, C391, C392		CCSRCH331J50
	C945, C946		CCSRCH331J50
	C109		CCSRCH391J50
	C297, C555		CCSRCH470J50
	C241		CCSRCH560J50
	C107, C360		CCSRCH681J50
	C489		CCSRCH8R0D50
	C123, C201, C233, C254		CEV101M16
	C368, C369, C413, C414		CEV101M16

Mark	No.	Description	Part No.
	C103		CEV220M16
	C205, C326, C401, C470, C472		CEV221M4
	C701, C711, C745, C752, C766		CEV221M4
	C781, C791, C793, C835, C891		CEV221M4
	C903, C908		CEV221M4
	C101		CEV470M6R3
	C116, C127, C223, C224, C264		CKSQYB105K10
	C312, C406, C407, C415, C416		CKSQYB105K10
	C477, C794, C795		CKSQYB105K10
	C216, C313, C351, C427, C531		CKSRYB102K50
	C533, C534, C606, C617, C621		CKSRYB102K50
	C703, C748, C831, C925, C926		CKSRYB102K50
	C951		CKSRYB102K50
	C110, C113, C203, C220, C225		CKSRYB103K50
	C234, C261, C320–C322, C330		CKSRYB103K50
	C404, C426, C619, C920		CKSRYB103K50
	C108, C111, C114, C115		CKSRYB104K16
	C212, C213, C227, C231		CKSRYB104K16
	C248–C251, C255, C263, C315		CKSRYB104K16
	C317		CKSRYB104K16
	C106		CKSRYB152K50
	C208		CKSRYB222K50
	C266		CKSRYB224K10
	C206, C214, C242, C357		CKSRYB472K50
	C105, C118, C122, C253, C256		CKSRYF104Z25
	C332, C353, C359, C365, C366		CKSRYF104Z25
	C609, C622, C631, C723, C755		CKSRYF104Z25
	C758, C761, C762, C767, C768		CKSRYF104Z25
	C836, C840, C848, C849		CKSRYF104Z25
	C895–C899, C902, C933, C939		CKSRYF104Z25
	C112, C125, C126, C130, C200		CKSRYF105Z10
	C202, C204, C215, C217		CKSRYF105Z10
	C221, C222, C226, C230, C232		CKSRYF105Z10
	C236, C258, C265, C299, C310		CKSRYF105Z10
	C319, C323, C328, C329, C409		CKSRYF105Z10
	C412, C418, C423, C428		CKSRYF105Z10
	C475, C476, C493, C494		CKSRYF105Z10
	C552–C554, C556, C602–C605		CKSRYF105Z10
	C607, C608, C610, C613–C616		CKSRYF105Z10
	C618, C657, C658, C704		CKSRYF105Z10
	C706–C710, C712–C716		CKSRYF105Z10
	C718–C722, C724–C732, C735		CKSRYF105Z10
	C741–C744, C746, C747		CKSRYF105Z10
	C753, C754, C756, C757		CKSRYF105Z10
	C759, C760, C763–C765		CKSRYF105Z10
	C769–C780, C782–C790, C792		CKSRYF105Z10
	C797, C832–C834, C837–C839		CKSRYF105Z10
	C842–C846, C893, C900, C901		CKSRYF105Z10
	C904–C907, C909–C918		CKSRYF105Z10
	C921–C924, C927–C930		CKSRYF105Z10
	C956, C957		CKSRYF105Z10
	C117, C128, C422 (100/6.3)		VCH1194
	C119, C421, C424, C601 (150/4)		VCH1195
	C623, C702, C751 (150/4)		VCH1195
	C403, C405 (47/16)		VCH1210
	C411, C419 (100/6.3)		VCH1211

RESISTORS

Mark	No.	Description	Part No.
	R831, R832		RAB4C0R0J
	R924–R927		RAB4C101J
	R631, R713		RAB4C103J
	R111		RAB4C220J
	R113, R534, R537, R704, R705		RAB4C470J
	R138		RS1/10S0R0J
	R341		RS1/10S101J
	R141–R148		RS1/10S220J
	R364, R369, R373, R375		RS1/16S1003F
	R123		RS1/16S1202F
	R843, R855		RS1/16S1501F
	R358, R361		RS1/16S1503F
	R755		RS1/16S1801F
	R936, R944, R950, R966, R973		RS1/16S3000F
	R978		RS1/16S3000F
	R754		RS1/16S3001F
	R751		RS1/16S3301F
	R132		RS1/16S4702F
	R357, R362, R363, R368, R372		RS1/16S6802F
	R374		RS1/16S6802F
	R257 (R=1.0)		VCN1127
	R258, R259 (R=2.2)		VCN1128
	Other Resistors		RS1/16S###J

OTHERS

CN401	PH CONNECTER	S13B-PH-SM3
CN103	CONNECTOR	S5B-PH-SM3
9006	FLEXIBLE CABLE	VDA1681
CN114	4P CONNECTOR	VKN1409
CN115	12P CONNECTOR	VKN1416
CN402	17P CONNECTOR	VKN1421
CN551	21P CONNECTOR	VKN1425
CN701	24P CONNECTOR	VKN1428
CN901	30P CONNECTOR	VKN1434
CN502	20P CONNECTOR	VKN1460
CN111	26P CONNECTOR	VKN1790
CN531	FFC CONNECT0R	VKN1794
KN1, KN2	EARTH METAL FITTING	VNF1109
X481 (27.000MHz)		VSS1159
X601 (16.5MHz)		VSS1160

C JACB ASSY

SEMICONDUCTORS

Mark	No.	Description	Part No.
	IC401, IC501		DSD1702EG
	IC701		LA73054
	IC302–IC305, IC402, IC502		NJM5532MD
⚠	IC102		NJM78M05FA
⚠	IC101		NJM78M08FA
	IC301		PCM1738EG-3
⚠	IC702		PQ05RD11
	IC201		TC74VHC157F
	IC202		TC7SH08F
	IC203		TC7SHU04F
	Q312, Q322, Q432, Q532, Q534		2SA1037K
	Q601, Q801, Q802		2SC2412K
	Q350, Q351, Q360, Q361, Q410		2SD2114K
	Q420, Q510, Q520		2SD2114K
	Q201, Q310, Q311, Q320, Q321		DTC114YK
	Q430, Q431, Q530, Q531, Q533		DTC114YK
	D701–D712, D801, D802		1SS355
	D380		UDZS6.2B

COILS AND FILTERS

Mark No.	Description	Part No.
	L701, L702 CHIP BEADS	VTL1089
CAPACITORS		
	C307, C406, C506	CCSRCH331J50
	C115, C116, C118–C120, C801	CCSRCH470J50
	C702, C721	CEAT101M16
	C701, C741, C742, C751, C753	CEAT102M6R3
	C761	CEAT102M6R3
	C725, C762, C763	CEAT471M6R3
	C110	CEHAZA471M6R3
	C605	CEJQ101M16
	C604	CEJQ1R0M50
	C411, C421, C511, C521	CKSRYB272K50
	C117, C407, C413, C423, C507	CKSRYF104Z25
	C513, C523, C704, C711–C716	CKSRYF104Z25
	C752, C754, C803	CKSRYF104Z25
	C111, C112, C114, C202, C204	CKSRYF105Z10
	C302, C403, C503, C601, C606	CKSRYF105Z10
	C703, C722–C724, C726, C805	CKSRYF105Z10
	C334, C336, C344, C346 (470P)	VCE1035
	C330, C331, C340, C341 (4700P)	VCE1046
	C310, C311, C320, C321 (2200P)	VCE1048
	C412, C422, C512, C522 (1608CH330P)	VCH1226
	C350, C360, C414, C424, C514 (C= 47)	VCH1236
	C524 (C= 47)	VCH1236
	C101, C103, C314, C324, C338 (C= 100)	VCH1237
	C372, C380, C401, C410, C416 (C= 100)	VCH1237
	C420, C501, C510, C516, C520 (C= 100)	VCH1237
	C107, C109, C201, C301, C303 (C= 330)	VCH1239
	C402, C502 (C= 330)	VCH1239
	C305, C306, C405, C505 (C= 47)	VCH1240
RESISTORS		
	R330, R331, R334, R335	RN1/16SE1001D
	R340, R341, R344, R345	RN1/16SE1001D
	R301	RN1/16SE1602D
	R310, R311, R320, R321	RN1/16SE2000D
	R410, R420, R510, R520	RN1/16SE2201D
	R332, R333, R342, R343	RN1/16SE3001D
	R411, R418, R421, R427, R511	RN1/16SE8201D
	R518, R521, R527	RN1/16SE8201D
	R1101	RS1/10S0R0J
	R751, R752, R754, R755	RS1/16S75R0F
	R757–R761	RS1/16S75R0F
	Other Resistors	RS1/16S###J
OTHERS		
	CN705 SOCKET	AKP7012
	JA602 OPT. LINK OUT	GP1FA502TZ
	JA801, JA802 JACK	RKN1004
	PCB BINDER	VEF1040
	JA302 JACK	VKB1125
	JA301 JACK	VKB1133
	JA703 JACK	VKB1135
	JA702 JACK	VKB1151
	JA601 JACK	VKB1160
	CN101 21P CONNECTOR	VKN1252
	CN701 30P CONNECTOR	VKN1261
	CN801 7P CONNECTOR	VKN1267
	CN102 19P CONNECTOR	VKN1775
	KN101, KN102 EARTH METAL FITTING	VNF1084

Mark No.	Description	Part No.
D SACDB ASSY		
SEMICONDUCTORS		
⚠	IC906	BA25BC0FP
	IC901	CXD2753R
	IC902	HY57V161610DTC-8
⚠	IC808	MM1561JF
	IC904	TC7SH00FU
	IC991	TC7SHU04F
	IC806	TC7SH04FU
	IC905	TC7WH74FU
	IC801	XCA56367PV150
COILS AND FILTERS		
	L801	LCYA1R0J2520
	L971–L979 CHIP BEADS	VTL1074
CAPACITORS		
	C903	CCSRCH100D50
	C950	CCSRCH102J50
	C931	CCSRCH470J50
	C801, C829, C839, C840, C844	CEJQ221M6R3
	C901, C909, C911, C922, C926	CEJQ221M6R3
	C944, C951	CEJQ221M6R3
	C828, C908, C916	CKSRYB103K50
	C827	CKSRYB473K25
	C807–C812, C815, C816	CKSRYF105Z10
	C819–C824, C826, C830–C837	CKSRYF105Z10
	C841, C843, C902, C905–C907	CKSRYF105Z10
	C912–C915, C917–C921	CKSRYF105Z10
	C923–C925, C927–C930, C934	CKSRYF105Z10
	C937, C938, C940, C943	CKSRYF105Z10
	C945–C947, C955, C956, C991	CKSRYF105Z10
RESISTORS		
	All Resistors	RS1/16S###J
OTHERS		
	PCB BINDER	VEF1040
	CN903 13P CONNECTOR	VKN1417
	CN801 20P CONNECTOR	VKN1460
	CN902 19P CONNECTOR	19R-1.25FJ
	CN901 FFC CONNECT0R	VKN1794
E FLKY ASSY		
SEMICONDUCTORS		
	IC101	PE5314B
	IC102	PST3228
	Q103, Q105	2SA1602A
	Q104	2SC2412K
	Q102	DTA124EK
	Q101	DTC124EK
SWITCHES AND RELAYS		
	S101–S106	ASG7013
CAPACITORS		
	C101, C103, C107, C108, C161	CCSRCH102J50
	C104	CEAL470M6R3
	C100	CEJQ101M6R3
	C111	CKSRYB103K50
	C116	CKSRYF104Z50
	C102, C105, C110, C113, C115	CKSRYF105Z10

Mark	No.	Description	Part No.
		RESISTORS	
		All Resistors	RS1/16S###J
		OTHERS	
	CN102	CONNECTOR 9P	09P-FJ
	IC103	REMOTE RECEIVER UNIT	SPS-452L-H
	V101	FL TUBE	VAW1073
		SPACER	VEC2220
	CN101	17P CONNECTOR	VKN1277
		HOLDER	VNF1122
	X101	(5MHz)	VSS1142

F KEYB ASSY

Mark	No.	Description	Part No.
		SEMICONDUCTORS	
	D205		NSPB500-0008
	D203, D204		SLR-343VC
	D211		UDZS6.2B
		SWITCHES AND RELAYS	
	S201–S203		ASG7013
		RESISTORS	
	All Resistors		RS1/16S###J
		OTHERS	
	CN201	CONNECTOR 9P	09R-FJ

G POWER SUPPLY UNIT

Mark	No.	Description	Part No.
		OTHERS	
⚠	P103	PROTECTOR(1.6A)	AEK7012
⚠	P101	PROTECTOR(800mA)	AEK7063
⚠	P102	PROTECTOR(1.6A)	AEK7066
⚠	P104	PROTECTOR(2A)	AEK7067
⚠	F1	FUSE(2A)	REK1101

I ILKB ASSY

Mark	No.	Description	Part No.
		SEMICONDUCTORS	
	IC203		BU2370FV
	IC204		NJU7093AF
	IC101		PD5787A
	IC301		TC74VHC541FT
	IC306, IC308		TC7SH04FU
	IC205, IC302, IC309		TC7SH08FU
	IC201		TSB43CA43GGW
	IC202		VYW2026
	D261		RB501V-40
		COILS AND FILTERS	
	L201–L204 (330uH)		VTH1043
		CAPACITORS	
	C421, C423–C425		CCSRCH101J50
	C208		CCSRCH102J50
	C205		CCSRCH150J50
	C204		CCSRCH180J50
	C283, C284		CCSRCH221J50
	C411		CEV101M16
	C231, C261, C270, C277		CEV470M6R3
	C404		CKSQYB102K50
	C403		CKSQYF105Z16
	C307, C422, C426		CKSRYB102K50
	C279		CKSRYB103K50
	C206		CKSRYB104K16
	C275, C278		CKSRYB105K6R3
	C274		CKSRYB683K16
	C152, C207, C210, C216, C219		CKSRYF104Z25
	C285, C286		CKSRYF104Z25
	C101, C103, C104, C151, C203		CKSRYF105Z10
	C209, C211, C213–C215		CKSRYF105Z10
	C217, C218, C220–C223, C232		CKSRYF105Z10
	C262, C271–C273, C276		CKSRYF105Z10
	C281, C282, C301, C302, C306		CKSRYF105Z10
	C308, C309, C402, C412		CKSRYF105Z10
	C102, C202, C212, C401, C405 (150/4)		VCH1195
		RESISTORS	
	R116–R119, R129, R220–R223		RAB4C0R0J
	R335, R339, R340		RAB4C0R0J
	R110, R212, R219, R256		RAB4C103J
	R349, R350, R353, R363		RAB4C103J
	R289, R290		RS1/16S5101F
	R281–R288		RS1/16S56R0D
	R206		RS1/16S6341D
	Other Resistors		RS1/16S###J
		OTHERS	
	X201 (24.5760MHz)		ASS7025
	CN103	07P CONNECTOR	RKN1048
	CN102	13P CONNECTOR	VKN1417
	CN101	24P CONNECTOR	VKN1428
	JA1, JA2	1394-TERMINAL	VKN1800
	X101	(6.14MHz)	VSS1179

6. ADJUSTMENT

6.1 ADJUSTMENT ITEMS AND LOCATION

■ Adjustment Items

[Mechanism Part]

❶ Tangential and Radial Height Coarse Adjustment

❷ DVD Jitter Adjustment

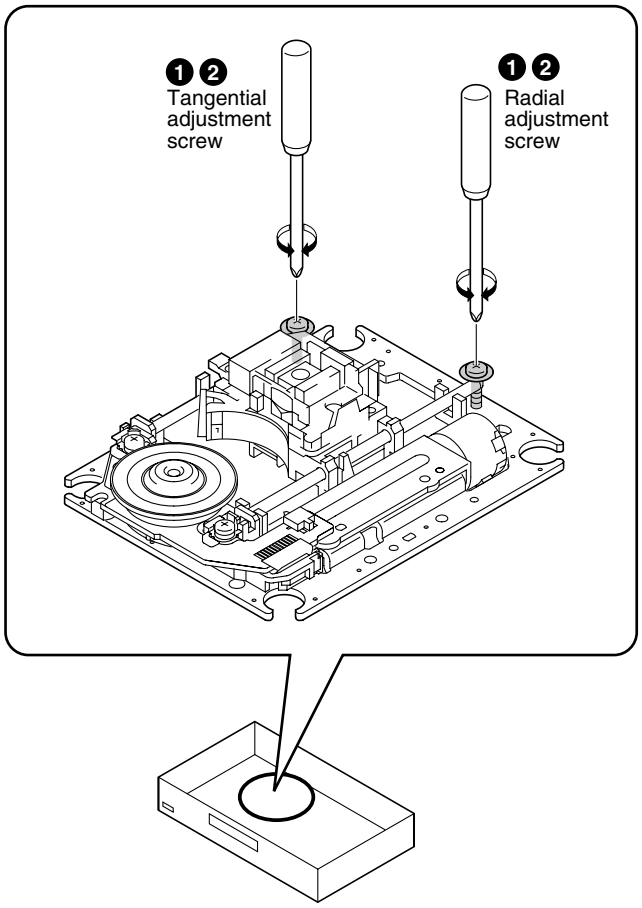
❸ Initialize the Focus Sweep Setting

[Electrical Part]

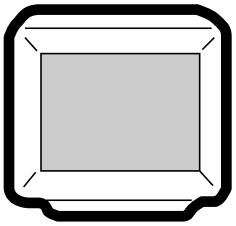
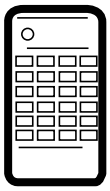
Electrical adjustments are not required.

■ Adjustment Points (Mechanism Part)

Cautions: After adjustment, adjustment screw locks with the Screw tight.



6.2 JIGS AND MEASURING INSTRUMENTS

 ⊕ Screwdriver (large)	 ⊕ Screwdriver (medium)	 TV monitor	 Test mode remote control unit (GGF1067)
 ⊕ Precise screwdriver	 DVD test disc (GGV1025)	Screw tight (GYL1001)	

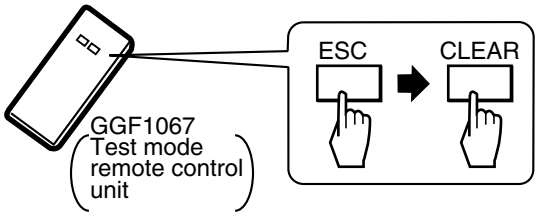
6.3 NECESSARY ADJUSTMENT POINTS

When	Adjustment Points	
■ Exchange Parts of Mechanism Assy		
Exchange the Pickup	Mechanical point	❶, ❷, ❸ ＊ After adjustment, screw locks with the Screw tight.
	Electric point	———
Exchange the Traverse Mechanism	Mechanical point	❸
	Electric point	———
Exchange the Spindle Motor	Mechanical point	❷, ❸ ＊ After adjustment, screw locks with the Screw tight.
	Electric point	———
■ Exchange PCB Assy		
Exchange PC Board LOAB, DVDM ASSY	Mechanical point	———
	Electric point	———

＊

Purpose: To set the sweep which was correct with the individual Traverse mechanism.

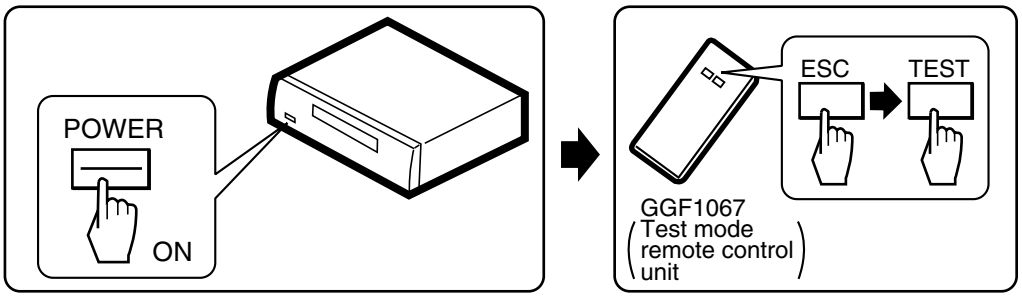
Be sure to perform the following step finally when replaced Pickup, Traverse Mechanism and Spindle Motor.



(It is necessary when performed adjustment procedure ❷.)

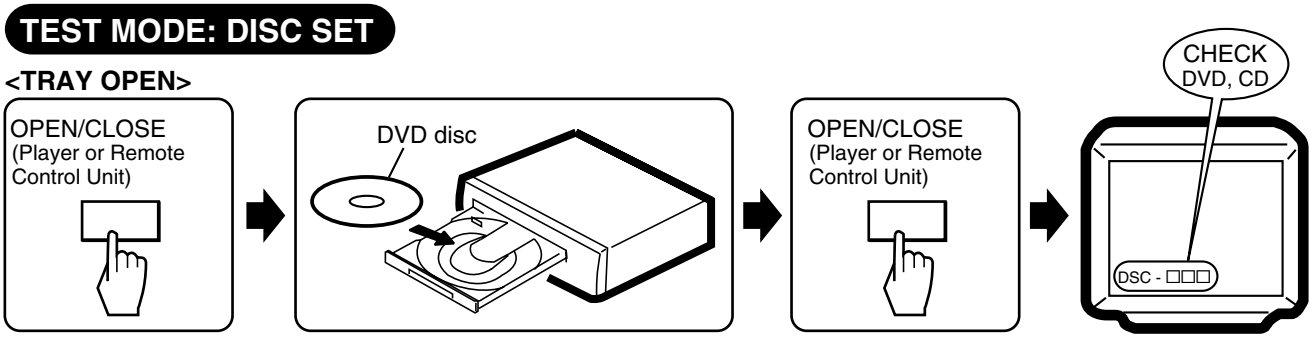
6.4 TEST MODE

TEST MODE: ON



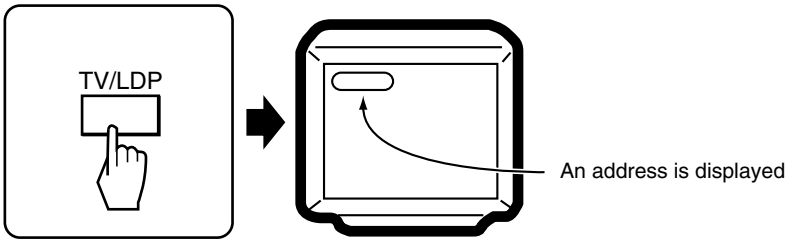
TEST MODE: DISC SET

<TRAY OPEN>



TEST MODE: PLAY

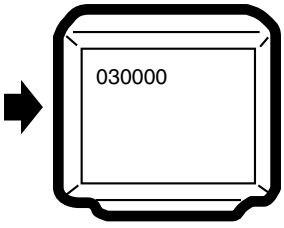
<PLAY>



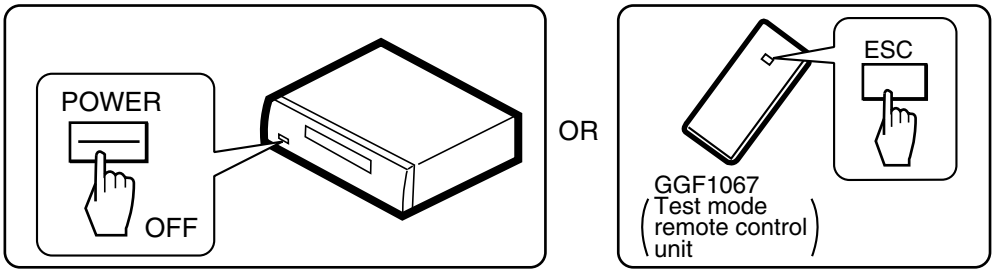
< When playback with the target address of disc (DVD)>

For example, when playback with # 30000

During PLAY [+10] ➡ [3] ➡ [0] ➡ [0] ➡ [0] ➡ [0] ➡ [CHP/TIM] Press keys in order



TEST MODE: OFF

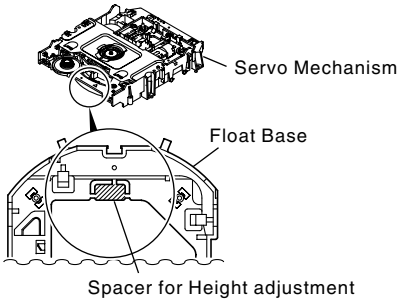


6.5 MECHANISM ADJUSTMENT

1 Tangential and Radial Height Coarse Adjustment

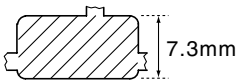
START

- Remove the servo mechanism.
- Remove a Spacer for height adjustment attached to the back side (shaded area) of the Servo Mechanism (Float Base) with nippers.

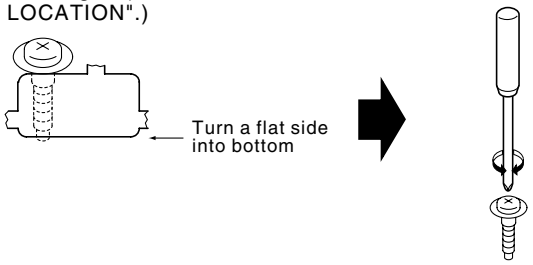


Note:
Turn the Short switch to Short side when removing the Pickup Flexible Cable. (Refer to "7.1.9 DISASSEBLY".)

Cautions:
Because there is not a Spacer for height adjustment in adjustment after the second time, will keep it at need. (This parts is Traverse mechanism exclusive use of a model for 2001 years)



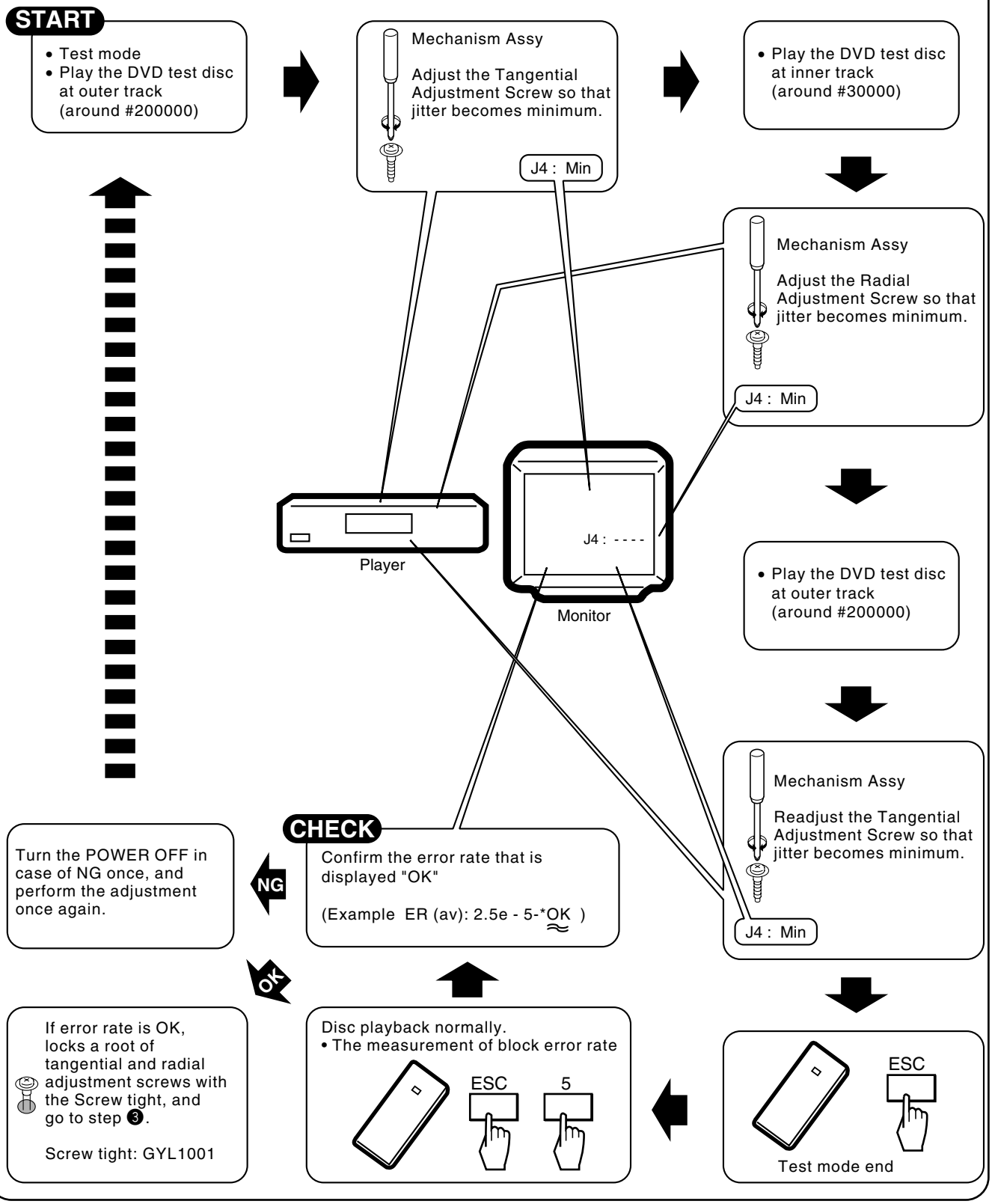
Put a spacer between a Tangential (or Radial) adjustment screw and Mechanism Base and turn each screw to adjust the height. (Refer to "6.1 ADJUSTMENT ITEMS AND LOCATION".)



❷ DVD Jitter Adjustment

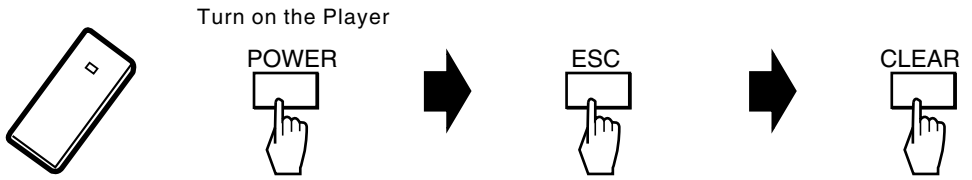
- Playback method of inner and outer address for the purpose is refererd to "6.4 TEST MODE".
- Jitter indication of the monitor is refererd to "7.1.3 TEST MODE SCREEN DISPLAY".

Use disc: GGV1025



❸ Initialize the Focus Sweep Setting

Purpose: To set the sweep which was correct with the individual Traverse mechanism.



Note: Be sure to perform this step when replaced the Pickup or Traverse mechanism.

7. GENERAL INFORMATION

7.1 DIAGNOSIS

7.1.1 ID NUMBER AND ID DATA SETTTING

Entering the ID Number and ID Data for Players with DVD-Audio and DVD-RW Compatibility

It is necessary with a player with DVD-audio and DVD-RW compatibility to set an individual number (ID number) and ID data. If the number and data are not set correctly with the following procedure, operations in the future may not be guaranteed. You will find the ID number to be set on the yellow label on the rear panel.

Important: If no yellow label is found on the rear panel, write down the specified ID number by checking it according to "How to confirm the ID number" shown below.

The Input is Necessary When:

- Downloading FLASH-ROM is finished. (The latest version must be downloaded when a repair is made.)
- "No ID Number" is displayed on the screen or FL display immediately after the power is turned on or in Stop mode.
- If "No ID DATA" is displayed, the ID data must be entered.

Note:
Be sure to enter the ID number in Stop mode.
Use the service remote control (GGF1067) for operations. Only opening/closing of the tray are performed from the player.
Use Disc No. : GGV1084

How to Input the ID Number and ID Data

① To enter the input mode, press ESC + STEREO in a status with no ID number set, such as after FLASH-ROM downloading.

↓

② As number input is enabled when the unit enters the input mode, input the 9-digit ID number.
(The entered number is also displayed on the FL display.)

```
[Player's ID Number Setting]
  ID Number ?
② > - - - - - - - - -

<CLEAR>  Exit


Input ID Number !
```

↓

③ After inputting the number, press SEARCH to register the ID number.

```
[Player's ID Number Setting]
  ID Number ?
> 0 0 0 0 0 0 0 0 1   OK ?

<PLAY>      Compare Mode
③ <SEARCH>  Enter

Input ID Number !
```

↓

④ When the ID number has been registered, the unit enters the ID data input mode. (The FL display indicates "NO ID DATA.") In this condition, place the ID data disc on the tray and close the tray using the CLOSE key "■/⏏" on the player.

```
[Player's ID Data Setting]


<CLEAR>  Exit


④ Insert The ID Data Disc !
```

↓

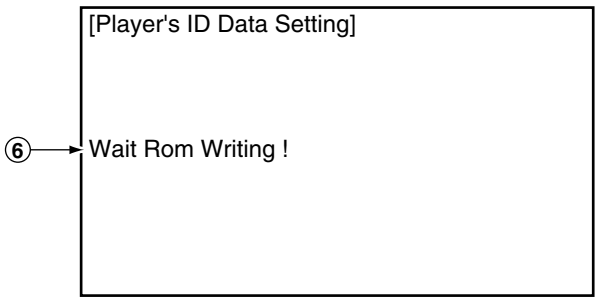
⑤ While the data are being read, the message shown in the figure at left is displayed on the screen.
(The FL display indicates "RD ID DATA.")

```
[Player's ID Data Setting]


⑤ Loading The ID Data Disc !
```

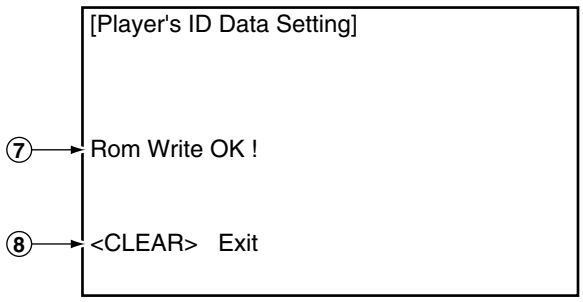
↓

⑥ When the ID data have been read, the data are written to the FLASH-ROM.
(The FL display indicates "WR ID DATA.")



⑦ When the ID data have been written to the FLASH-ROM, the message "Rom Write OK" is displayed on the screen.
(The FL display indicates "ID DATA OK.")

⑧ After confirming this message, press CLEAR to exit the input mode.

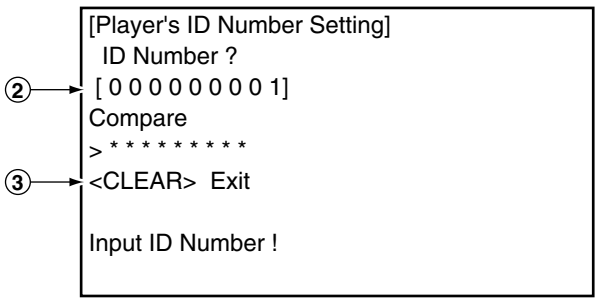


How to Confirm the ID Number

① Press ESC + STEREO with an ID number set, and the unit enters the ID number confirmation mode.

② The set ID number is displayed on the screen (and on the FL display), permitting you to confirm it.

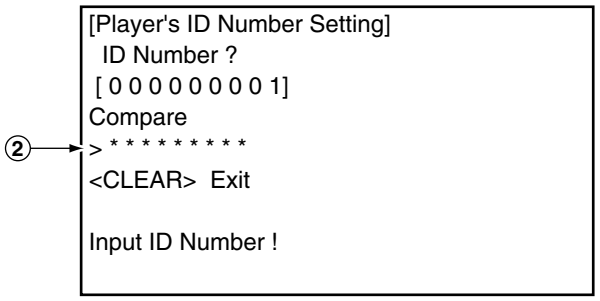
③ To exit this mode, press CLEAR.



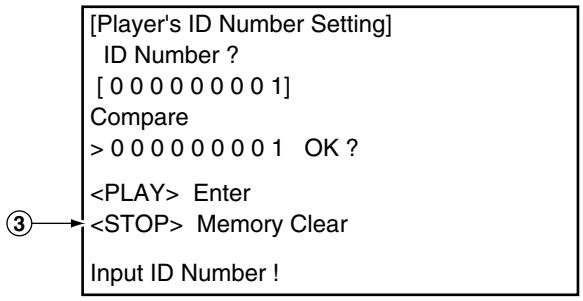
How to Clear the ID Number

① Press ESC + STEREO with an ID number set, and the unit enters the ID number confirmation mode.

② Input the same number as the ID number you have set.



③ After inputting the number, press STOP.
Only when the entered number matches the set ID number, the ID number is cleared and the unit exits this mode.
If the numbers do not match, you must return to step 2.
(STOP is not accepted until 9 digits are entered.)



7.1.2 SELF-DIAGNOSIS FUNCTION OF PICKUP DEFECTIVE

This unit can confirm the laser diode current value (DVD: 650nm, CD: 780nm) of pickup on the Test Mode screen.
(Press the [ESC] → [TEST] keys in order on the test mode remote control unit (GGF1067) to enter the test mode.)

It's effective in case of the following condition.

Symptom

- Indicates "No Disc" in FL display.
- Player does not playback, etc..

Procedure of Self-Diagnosis

① Enter the Test mode.

② When diagnosing the 650nm laser diode:
Press the [TEST] → [1] keys in order, and turn on the laser diode (It light-up for nine seconds.).
When diagnosing the 780nm laser diode:
Press the [TEST] → [4] keys in order, and turn on the laser diode (It light-up for nine seconds.).

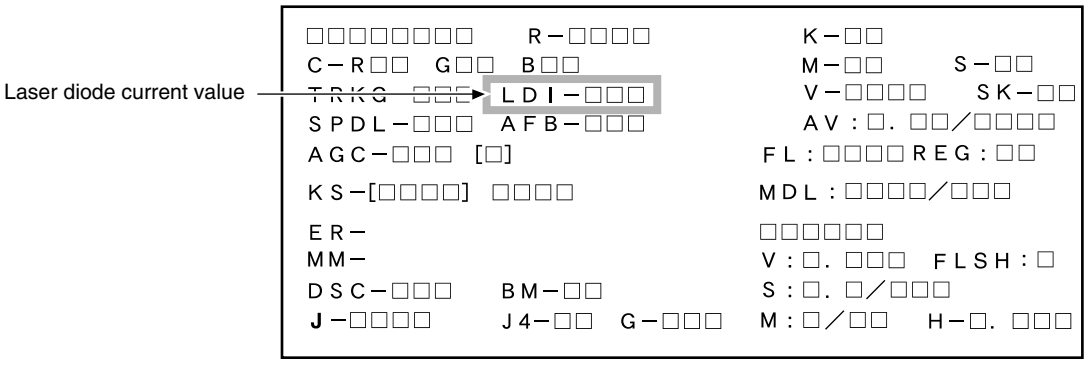
(When let it turn on once again after performed ② once,
After pressed [REP.B] key once
650nm: Press the [TEST] → [1] keys in order
780nm: Press the [TEST] → [4] keys in order)

③ Confirm the indicated value of the laser diode current (LDI). (Refer to following figure.)

④ **When indicated value is more than 100, pickup is defective. → Replacement is necessary**
Replace the Traverse Mechanism Assy or Pickup.

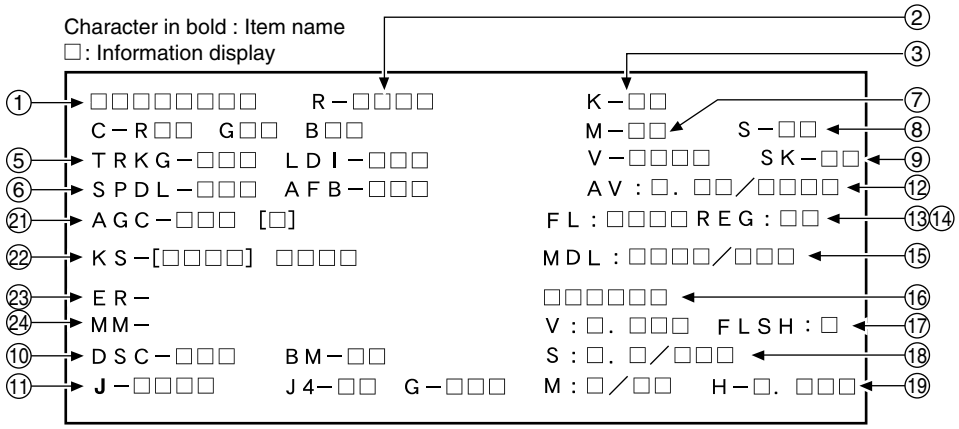
Note : When a DVD disc or a CD disc is played in the test mode, this function is effective.

Character in bold : Item name
□: Information display



7.1.3 TEST MODE SCREEN DISPLAY

■ Display Specification of the Test Mode



① **Address indication**
The address being traced is displayed in number.
(as for the DVD, indication of decimal number is possible.)
DVD : ID indication (hexadecimal number, 8 digits)
[＊＊＊＊＊＊＊＊]
CD : A-TIME (min. sec.) [0 0 0 0 ＊＊＊＊]

② **Code indication of remote control unit [R – ＊＊＊＊]**
In case of double code, display a 2nd code.

③ **Main unit keycode indication [K – ＊＊]**

④ **Background color indication [C – R＊＊ G＊＊ B＊＊]**

⑤ **(1) Tracking status [TRKG – ＊＊＊]**
Tracking on : [ON]
Tracking off : [OFF]
(2) Laser diode current value [LDI – ＊＊＊]

⑥ **(1) Spindle status [SPDL – ＊＊＊]**

Spindle accelerator and brake, free-runnimg	[A/B]
FG servo	[FG]
Rough, velocity phase servo	[SRV]
Offset addition, rough, velocity phase servo	[O_S]

(2) AFB status [AFB – ＊＊]

ON	[ON]
OFF	[OFF]

⑦ **Mechanism (loading) position value [M – ＊＊]**
Unknown : [01] or [41]
Open state : [04]
Close state : [08]
During opening : [12]
During closing : [22]

⑧ **Slider position [S – ＊＊＊＊]**
CD TOC area : [IN]
CD active area : [CD]

⑨ **Output video system [V – ＊＊＊＊]**
NTSC system : [NTSC]
PAL system : [PAL]
Automatic setting : [AUTO]
Scart terminal output [SK – ＊＊]
(Display only the WY model which can do the output setting of scart terminal.)
VIDEO : [00]
S-VIDEO : [01]
RGB : [02]

⑩ **(1) Disc sensing [DSC – ＊＊＊]**
The type of discs loaded is displayed.
[DVD], [CD], [VCD], [ ]
(2) CD 1/3 beam switch [BM – ＊＊]

⑪ **Jitter value [J – ＊＊＊＊]**
Make the jitter four times, and renew it in every 0.5 second.
[J4 – ＊＊]

⑫ **Version of the AV-1 chip / version of firmware [AV: ＊＊ / ＊＊＊＊＊＊＊＊]**

⑬ **Version of the FL controller [FL: ＊＊＊＊]**

⑭ **Region setting of the player [REG: ＊]**
Setting value : [1] to [6]

⑮ **Destination setting of the FL controller [MDL: ＊＊＊＊ / ＊＊＊]**
Four characters in the front represent the type of model.
Three characters in the back represent the destination code.
J: /J, K: /KU, /KC, /KU/KC, R: /RAM/RL/RD, LB: /LB, WY: /WY

⑯ **Part number of the flash ROM and system controller [＊＊＊＊＊＊ / ＊＊＊＊＊＊]**

⑰ **Version of the flash ROM [V: ＊. ＊＊＊]**
Flash ROM size [FLSH = ＊]

⑱ **Revision of the system controller [S: ＊ . ＊ / ＊＊＊]**

⑲ **(1) Revision of the DVD mechanism controller [M: ＊/＊＊]**
(2) Part number of the GUI-ROM (OEM model) [GUI: ＊＊＊]
(3) HOST conversion [HOST: ＊＊＊]

㉑ **AGC setting [AGC – ＊＊＊ [＊]]**
AGC on : [AGC-ON]
AGC off : [AGC-OFF]
[1] : RFAGC on [0] : RFAGC off

㉒ **FTS servo IC information**
DSP coefficient indication [KS – [＊＊＊＊] ＊＊＊＊]
Displays the address (four digits) of the specified coefficient and the setting value (four digits) with [TEST] and [9] keys.

㉓ **Error rate indication**
① C1 error value of CD [ER – C1 ＊＊＊＊]
② C1 error value of DVD [ER – ＊＊＊＊ ＊＊＊＊]

㉔ **Internal operation mode of mechanism controller [MM – ＊＊ : ＊＊]**
Internal mechanism mode (2 digits) and internal mechanism step (2 digits) of the mechanism controller

7.1.4 SELF-DIAGNOSIS FUNCTION

When enter the service mode, self diagnosis mode operates with the "ESC"+"CHP/TIM" keys automatically.

① Mechanism Error History (past eight times of error is displayed)

Two columns of the beginning display the error status for mechanism controller.
(the details of error contents refer to "7.1.4 Error Display".)
Eight columns of the back display the count UP value (turned count up every 20msec) from the power-up.
Example) 32h ≒ 1 sec, BB8h ≒ 1 min, 2BF20h ≒ 1 hour
In addition, when there was error after power-up immediately (till initial setting is completed), turn the most significant bit to ON.

② Check Item Display of Self Diagnosis Function

a) AV1 Host Bus check (possible the check only during stop) (Read & Write process of an internal specific register)
AV_1 : OK
: —— ⇒ not yet check
: HOST BUS NG ⇒ HOST bus NG

b) Bus check between AV1 SDRAM (possible the check only during stop) (Read & Write process to the SDRAM)
AV_2 : OK
: —— ⇒ not yet check
: AV1-SDRAM BUS NG ⇒ Bus NG between AV1 and SDRAM

c) DMA transfer port check from F.E. to AV1 (during stop, possible the check only in DVD or NO DISC)
(writing from F.E to SDRAM and reading of SDRAM)
AV_3 : OK
: —— ⇒ not yet check
: FE-AV1 DMA NG ⇒ Bus NG between F.E and SDRAM installed outside of AV1

d) Video encoder (ADV****) check (Read of the specific register)
VE : OK
: NG ADV, ⇒ ADV register reading NG
: NG > ADV, ⇒ ADV communication NG of FR to video encoder
: NG > PRO ⇒ Communication NG from EBY to progressive decoder

e) DSP check (Read of the specific register)
DSP : OK
: NG ⇒ DASP NG

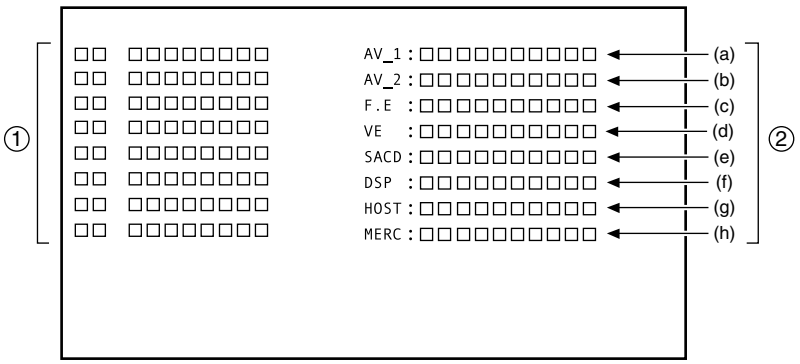
f) SACD check (Read of the specific register)
SACD : OK
: NG ⇒ SACD NG

g) 1394 relation HOST controller check
HOST : OK
: NG ⇒ HOST controller NG

h) 1394 relation Mercury CHIP check
MERC : OK
: NG ⇒ Mercury CHIP NG

Display the mechanism error history and self diagnosis result by pressing the "CHP / TIM" key once again.
Afterwards press the "CHP / TIM" key with toggle and change the display.

Display screen of mechanism error history and self diagnosis result



7.1.5 FUNCTION SPECIFICATION OF THE SERVICE MODE

• FL indication of EDC / ID error (short cut function)

Indicate it in FL with the "ESC"+"CX" keys (LD remote control unit).
Indication is released with the "ESC" key during display.

FL indication contents

00 / 00 / 01 ∗

- 01: Indicate number of the location that caused EDC and ID errors
- 00: Retry number of times at having caused ID error (error is indicated only in the occurring moment)
  Retry number of times of the latest ID error in the ST system
- 00: Retry number of times at having caused EDC error (error is indicated only in the occurring moment)
  Retry number of times of the latest EDC error in the ST system

∗ Mark: When even once causes AV1 error, lights.

• Screen display of the service mode

Indicate to the screen with the "ESC"+"CHP/TIM" keys.
Release the indication with the "ESC" key.
Indication contents

① ID Address

② DVD in playback: Error rate regular indication and exponent indication
CD/VCD in playback indicates the number of correct frame of C1 error /5 seconds.

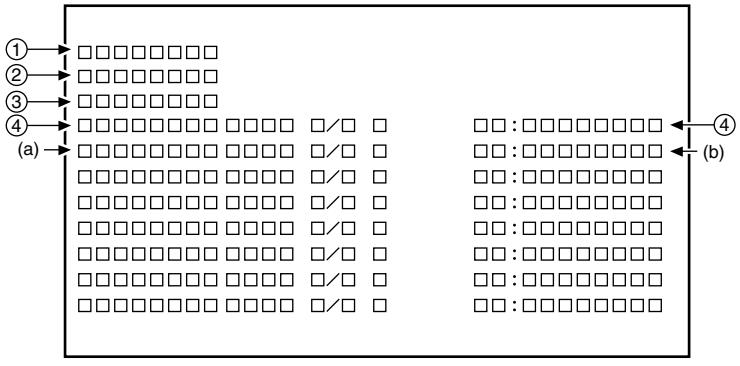
③ Self diagnosis indication
Indicate the self diagnosis result whether the F.E is normal.
Self Check : During FE checks
Self Check OK : Abnormality is not found in F.E.
Self Check Error : Abnormality is found in F.E.
Indicate the mechanism error history and self diagnosis result by pressing the "CHP / TIM" key once again.
Afterwards press the "CHP / TIM" key with toggle and change the display.
Indication of the mechanism error history and self diagnosis result refer to "7.1.1 self diagnosis function".

④ Error information indication of the AV decoder
(a)
When a retry occurred in reading from the disc, a history indicates the occurrence location and the occurrence reason.
History is indicated to past seven times.
Eight columns of the beginning show the physical address which occurred of retry.
As for four columns of next, bitmap indicates EDC status. LSB shows the first sector during a block and MSB shows a last sector.
Following field indicates the retry number of times.
One digit in front of " / " shows number of times of the retry by EDC Error which occurred in the same block in succession.
One digit after " / " shows number of times of the retry by ID Check Error which occurred in the same block in succession.
" * " of last one digit shows the EDC Check NG Count Over.
" # " shows the ID Check NG Count Over.
When " * " and " # " are not indicated, show that data were rightly readable by retry process.
(b)
Indicate the error information that detected with the Audio/Video Decoder. When error occurred, a history indicates the occurrence time and the occurrence reason. History is indicated to past seven times.
Field in front of ":" indicates the error information of Audio/Video Decoder.
(Indication information is different from Fujitsu Decoder with Mitsubishi Decoder)
02 model is 656 series and 757 series is Mitsubishi model.

• Specification for the Audio/Video Decoder (M65773FP) model of Mitsubishi
bit7: VLD Fatal Error detection
bit6: VLD Not Fatal Error detection
bit5: Number of Macro Block mismatch
bit4: Decode error
bit3: VLD Sequence Layer Fatal Error detection
bit2: VLD Picture Layer Fatal Error detection
bit1: VLD Slice Layer Fatal Error detection
bit0: Start-up Sequence Time-out Error detection
Following field in " : " indicates a value of STC (System Time Clock) which detected the above Audio/Video Decoder error.

∗ When often perform the switch of debug screen, an error history will be increased.
As for this, CPU power is used for update of OSD drawing, symptoms occur so that control of VBR Buffer is not in time.

Indication contents



7.1.6 ERROR DISPLAY

Error codes that are displayed on the FL display without using the remote control unit

FL Display	Possible causes	Operation of the unit
AV1 VER	AV-1 chip is not a match with the program of system controller	The sound may not out with the specific audio.
CPU AERR	CPU address error (Hardware is unusual.)	No operation
DMA AERR	DMA address error (Hardware is unusual.)	No operation
FLASH ID	Difference in versions of the internal ROM of the system controller and of the flash ROM, or bus line failure or reverse installation	No operation
FLASH WRP	Write protect error of the flash ROM	No operation
FLASH SIG	Difference in part number of the flash ROM (When the ROM which could't be used was used.)	No operation
FLASH SUM	Check sum error of the flash ROM (It exceeds the regular size.) or reverse installation (Hardware is unusual.)	No operation
FLASH SIZ	Size error of the flash ROM (Use 4 or 8 M-bit.)	No operation
GUI ROM ERROR	Difference in version of GUI ROM and system controller software.	Operate as the OSD model
ILLGAL	The system controller fetched a code other than an operation code (Hardware is unusual.)	No operation
MECHA CPU	Difference in version of the internal ROM of the mechanism controller and of the flash ROM.	No operation
RESERVE	Undefined interrupt (Hardware is unusual.)	No operation
SLOT	Inappropriate slot command issued (Hardware is unusual.)	No operation

Error codes that are displayed on the FL display by using the remote control unit (Mechanism controller error)

To display: ESC + DISPLAY + DISPLAY; Location of the display: At the two digits of center of the FL display
To display the error history: ESC + DISPLAY + One shot; Location of the display: TV screen

FL	Description of Error	Causes if with a DVD	Causes if with a CD	Operation of the Unit
11	Search timeout	Search could not be complete within 7 seconds.	Search could not be complete within 7 seconds, and it could not enter the target area within 7 seconds by VCD scan.	CD : Stops, DVD: Continues operation
12	Search retry error	More beyond the target while the read-in search was converging. A search could not be completed after 3 retries while the unit was tracing 11 tracks. A search could not be completed after retry when timeout occurs at read-in.		CD: Stops, DVD: Continues operation
19	Tracing timeout while converging	Timeout (10.5 seconds) while tracing at the stage of convergence of a search.		Stop
1B	Index 0 search error		During Track (Index) Search, the search for the beginning of a program could not be completed within 3 seconds (20 seconds in the case of Index Search) after positioning based on the TOC data was completed.	Stop
1C	Embossment plunge error (only a model corresponding to RW)	Plunged into unreadable embossment of DVD-RW player.		1. In wobble nothing (error distinction) : search to address 2E400h 2. In wobble existence: Tray open
22	Timeout of slider inner circumference	Inside switch could not ON within 3 seconds.		Stop
23	Timeout of slider outer circumference	Inside switch could not OFF within the following times: at ATB: 2 seconds, at Backup: 2 or 2.02 seconds.		Stop
33	No FOK pulse during playback	When the focus was deviated continuously 20 times.		Adjusts focus at the innermost circumference and tries to return to its position where the error was generated (for 3 times),then opens. If the same error persists after one retry, the tray opens. (No FOK pulse)
38	Disc-type-sensing error	Were not able to playback from the disc distinction process. PLAY or STOP was not completed by backup operation of the disc distinction. Distinguished it from the blank disc in the ATB process completion.		Open

FL	Description of Error	Causes if with a DVD	Causes if with a CD	Operation of the Unit
39	SGC converge timeout	SGC could not converge during detects the peak		Open
41	Spindle timeout	The unit did not enter Stop mode within 10 seconds of issuance of a Stop command. Disc distinction is not completed even if passes for 10 seconds after the spindle turned.		Stop
48	Spindle FG transition timeout	Did not reach to the rotating speed that ATB was possible for less than 10 seconds. Did not reach aim CAV lock speed (high: 10%, low: 50%) for less than 10 seconds. CAV process passed more than 5 seconds or abnormal speed was detected. Spindle does not lock for less than 3 seconds in the BCA read start or end.		Stops. (FG timeout)
49	Spindle PLL transition timeout	CAV process passed more than 5 seconds. Abnormal speed was detected.		Stops. ("73" is displayed during starting process.)
4A	Spindle lock timeout	Spindle could not lock more than 1.5 seconds before start the AFB.		Stops. ("73" is displayed during starting process.)
51	Auto sequence timeout of peak detection	ABUSY did not return within 1 second after the DDTCT (peak detection) command was sent.		Stop
52	Auto sequence timeout of focus jump down	ABUSY did not return within 30 mS after the FJMPD (Focus jump 1 to 0) command was sent.		Open
53	Auto sequence timeout of focus jump up	ABUSY did not return within 30 mS after the FJMPU (Focus jump 0 to 1) command was sent.		Open
54	Auto sequence timeout of play AGC	ABUSY did not return within 50 mS after the GSUMON (play-AGC-measuring) command was sent.		Stop
55	Auto sequence timeout of disc-type-sensing	ABUSY did not return within 2 seconds after the DJSRT (disc-sensing) command was sent.		Stop
56	Auto sequence timeout of ATB2	ABUSY did not return within 1 second after the TBLOFS (Internal ATB after the completion of external ATB) command was sent.		Stop
57	Auto sequence timeout of tracking servo ON	ABUSY did not return within 0.5 sec. after the TSON (tracking servo ON) command was sent.		Stop
58	Auto sequence timeout of ATB1	ABUSY did not return within 0.2 sec. after the TBL (external ATB) command was sent.		Stop
59	Auto sequence timeout of focus gain adjustment	ABUSY did not return within 2 seconds after the FGN (focus gain adjustment) command was sent.		Stop
5A	Auto sequence timeout of tracking gain adjustment	ABUSY did not return within 2 seconds after TGN (tracking gain adjustment) command was sent.		Stop
5B	Auto sequence timeout of offset adjustment	ABUSY did not return within 1 second after the AVE (offset adjustment) command was sent.		Stop
5C	Auto sequence timeout of modulation factor measurement	ABUSY did not return within 200 mS after the ADJMIR (modulation factor measurement) command was sent.		Stop
5D	Auto sequence timeout of auto focus bias	ABUSY did not return within 2 seconds after the AFB (auto focus bias) command was sent.		Stop
5F	Auto sequence already busy	A command could not be sent because ABUSY was low. ABUSY did not return within 200 mS after TLV command was sent.		Stop
62	Pause retry error	Pause mode could not be restored within three retries after it had been released.		Continues operation
71	ID reading check during playback	An ID could not be read for 1 second or more.		Stop
72	Subcode check failure during playback		No frame could be read for 3 seconds or more.	Stop
73	ID can not read during startup	An ID could not be read within 1 second after the AFB tracking on.		Opens (ID readout failure)

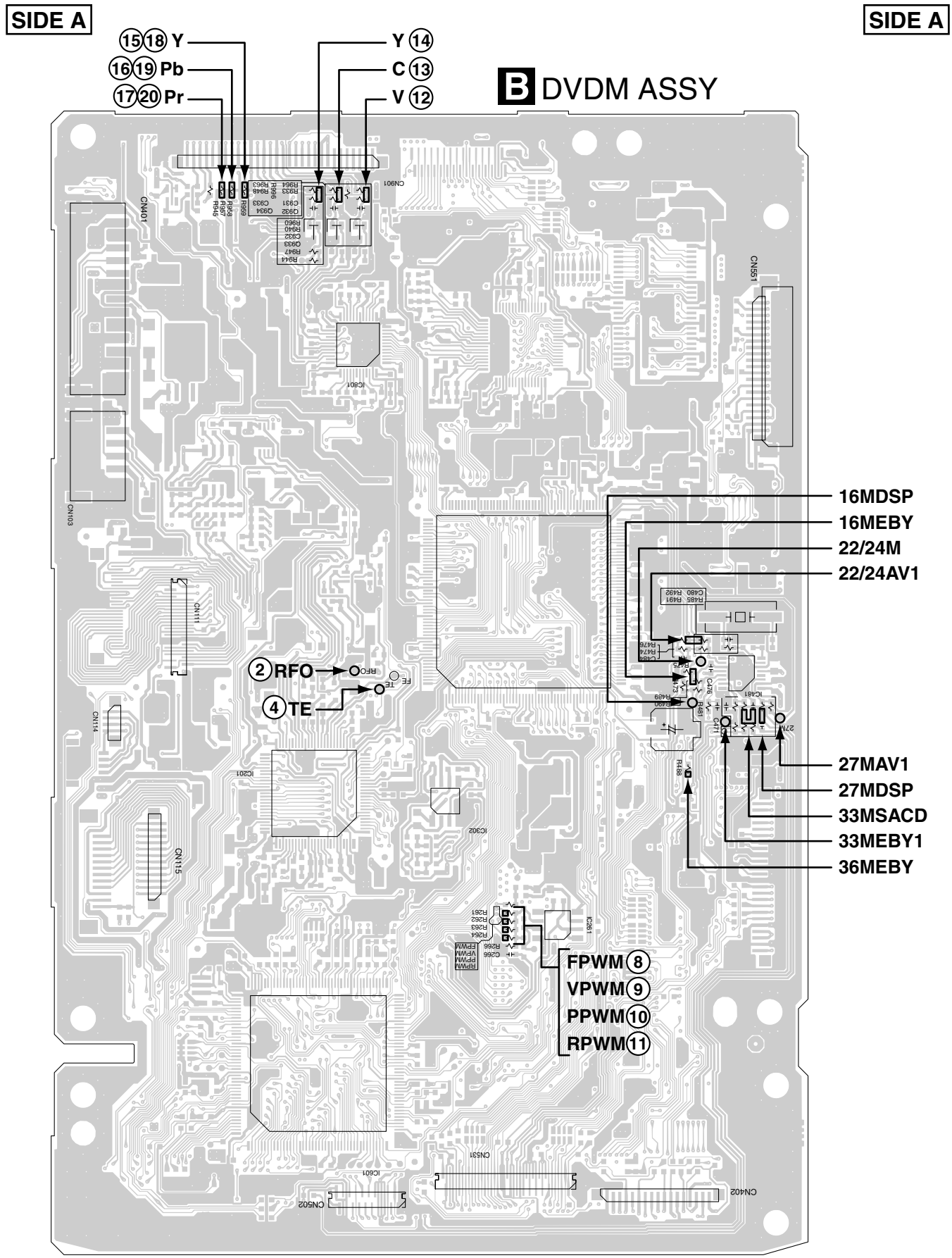
FL	Description of Error	Causes if with a DVD	Causes if with a CD	Operation of the Unit
74	Subcode check failure during startup		Subcode could not be read within 1 second after the tracking on.	Opens (Subcode readout failure).
A1	Communication timeout of DSP command	A command could not be issued to DSP because Command Busy (XCBUSY) was in force (XCBUSY = L) for a specified time (about 200 µS).		Open
A2	Communication timeout for reading DSP coefficient	Command Busy (XCBUSY) was in force for a specified time (about 200 µS) before and after a coefficient read command was issued to DSP, or the address echo-back after command issuance did not match the setup address.		Open
A4	Communication timeout for continuously writing DSP coefficient	Command Busy (XCBUSY) was in force for 200 µS during continuous coefficient writing, or before and after a continuous write command was issued to DSP.		Open
B1	Timeout error for backup	In the backup sequence, codes could not be read for fixed time.		Stops
B2	Retry error for backup	Cannot close tracking even if performs backup fixed number of times.		Stops
B3	Retry error for trace	During tracing, do not restore after the runaway detection backup was performed several times.		Stops
C3	Detection of tracking overcurrent	During playback, the overcurrent detection port was at L for 300 ms or more continuously.		Stops (the mechanical controller operates independently).
(C5)	Short-circuit test corresponding error	After the overcurrent detection (C3 error), furthermore the overcurrent detection port was at L for 300 mS or more continuously.		Turns off the power instantly (No indication on the FL display and no writing to flash memory)
F5	Tray being pushed	The tray switch that had been Open mode was forcibly changed to a mode other than Open by an external force.		Closes
F6	Code reading NG		(PH code nothing) When Philips code is not readable during LD starting, and a code was not readable after the slider moved to FWD and REV directions slowly each for five seconds. (PRD) In the CD starting, when a subcode of TOC part was not readable, but the subcode of the program area was readable.	Search, scan and special playback prohibition, Playback as playback CD-R (PRD mode) as it is.
F8	Loading timeout	Loading or unloading could not be completed within a specified time (about 10 seconds). Though a portable cover is opening, when a close command was issued from the system controller.		Reverses the loading direction. It timeout is repeated upon retry, the unit stops.
FC	Focus	• Focus ON sequence could not be completed more than two seconds. • Auto sequence command was finished, actually focus ON was not completed. • Focus did not enter even if retried it eight times.		Stops wherever possible then opens (stops in the case of side B).

Error codes that are displayed on the FL display by using the remote control unit (Device error)

To display: ESC + DISPLAY + DISPLAY; Location of the display: At the two digits of left of the FL display

FL	Description of Error	Causes if with a DVD	Causes if with a CD	Operation of the Unit
bit4=1 10 etc.	Mechanism controller RAM check sum error			No operation or it becomes debugging indication if the power is able to ON.
bit3=1 08 etc.	AV1 access error (read, write NG)			
bit2=1 04 etc.	LSI11 access error			
bit0=1 01 etc.	SRAM access error			

7.1.7 TEST POINTS LOCATION & WAVEFORMS



WAVEFORMS

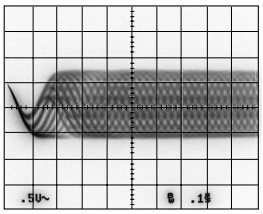
Note : The encircled numbers denote measuring point in the schematic diagram.

B DVDM ASSY

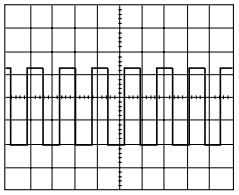
Measurement condition : No. 2, 4 and 8 to 11 : MJK1, Title 1-chp 1

No. 12 to 14 : DVD-REF-A1, T2-Chap.1
No. 15 to 20 : DVD-REF-A1, T2-Chap.19

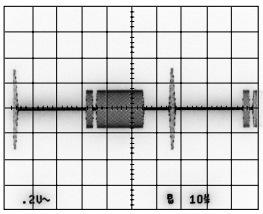
(2) Q106-emitter (RFO)
V: 500mV/div. H: 0.1µsec/div.



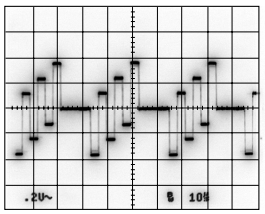
(8) Foot of R261 (FPWM)
V: 1V/div. H: 10µsec/div.



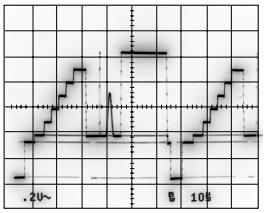
(13) Foot of R963 (C)
V: 0.2V/div. H: 10µsec/div.



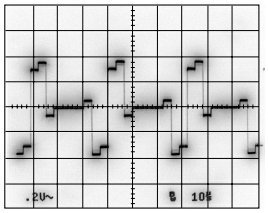
(19) Foot of R958 (Pb)
V: 0.2V/div. H: 10µsec/div.



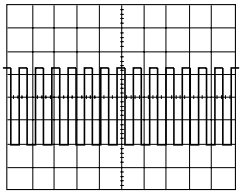
(14) Foot of R960 (Y)
V: 0.2V/div. H: 10µsec/div.



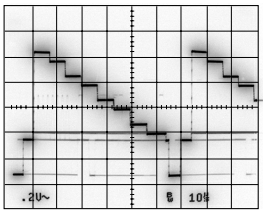
(20) Foot of R957 (Pr)
V: 0.2V/div. H: 10µsec/div.



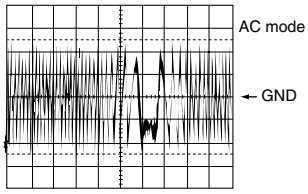
(9) Foot of R262 (VPWM)
V: 1V/div. H: 10µsec/div.



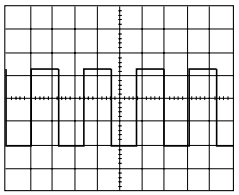
(15) Foot of R959 (Y)
V: 0.2V/div. H: 10µsec/div.



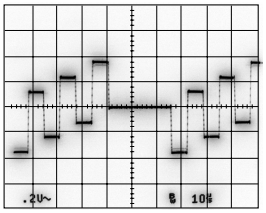
(4) IC101-pin 42 (Tracking Error) (AI-Inner Tracking Off)
V: 500mV/div. H: 2msec/div.



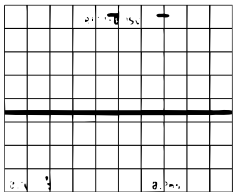
(10) Foot of R263 (PPWM)
V: 1V/div. H: 0.2msec/div.



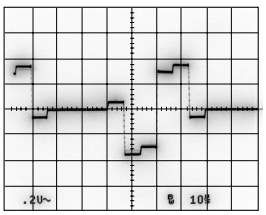
(16) Foot of R958 (Pb)
V: 0.2V/div. H: 10µsec/div.



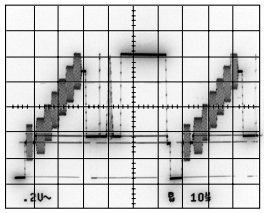
(11) Foot of R264 (RPWM)
V: 1V/div. H: 5msec/div.



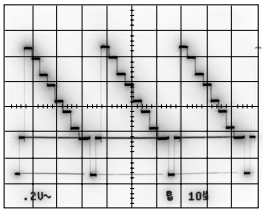
(17) Foot of R957 (Pr)
V: 0.2V/div. H: 10µsec/div.



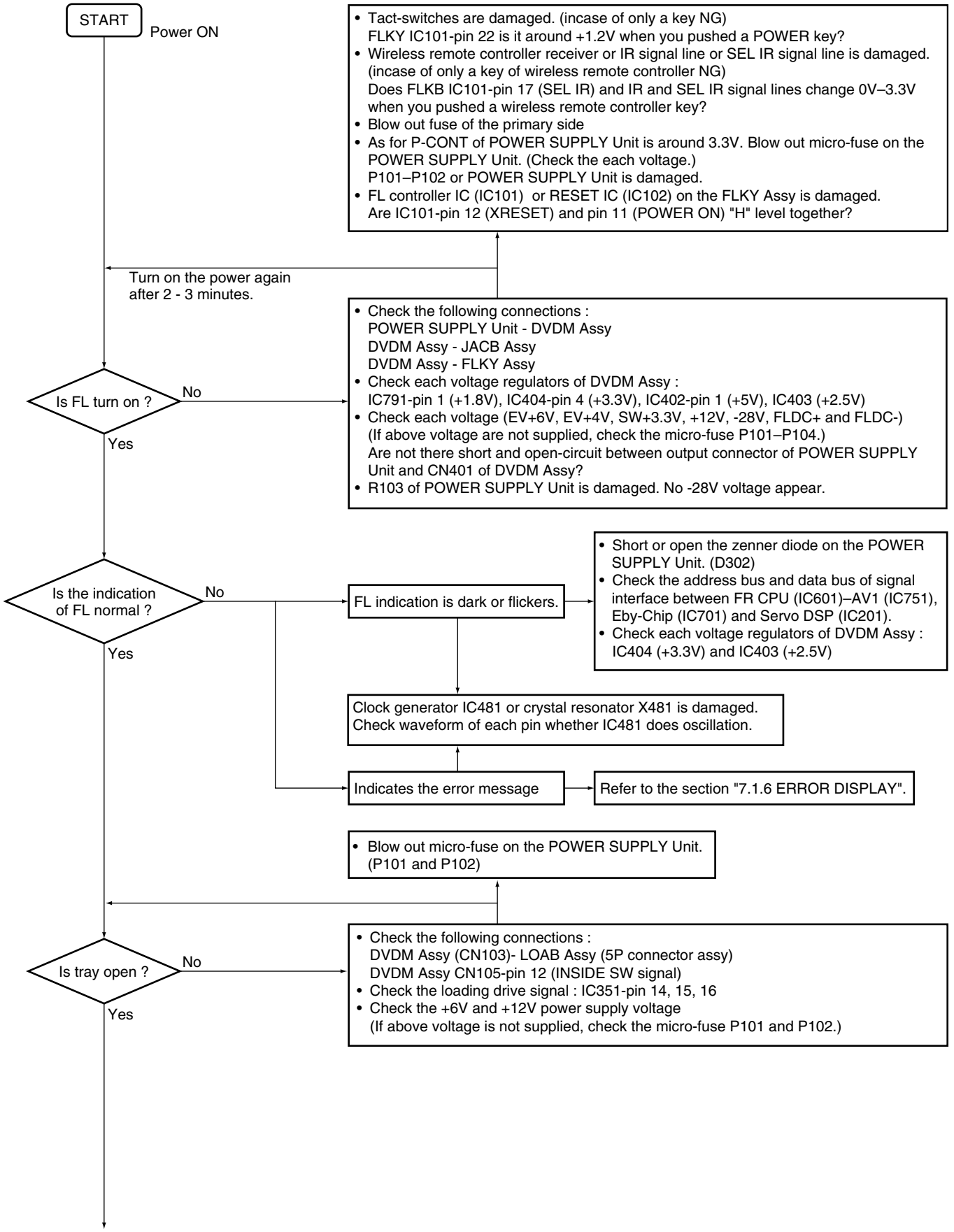
(12) Foot of R964 (V)
V: 0.2V/div. H: 10µsec/div.

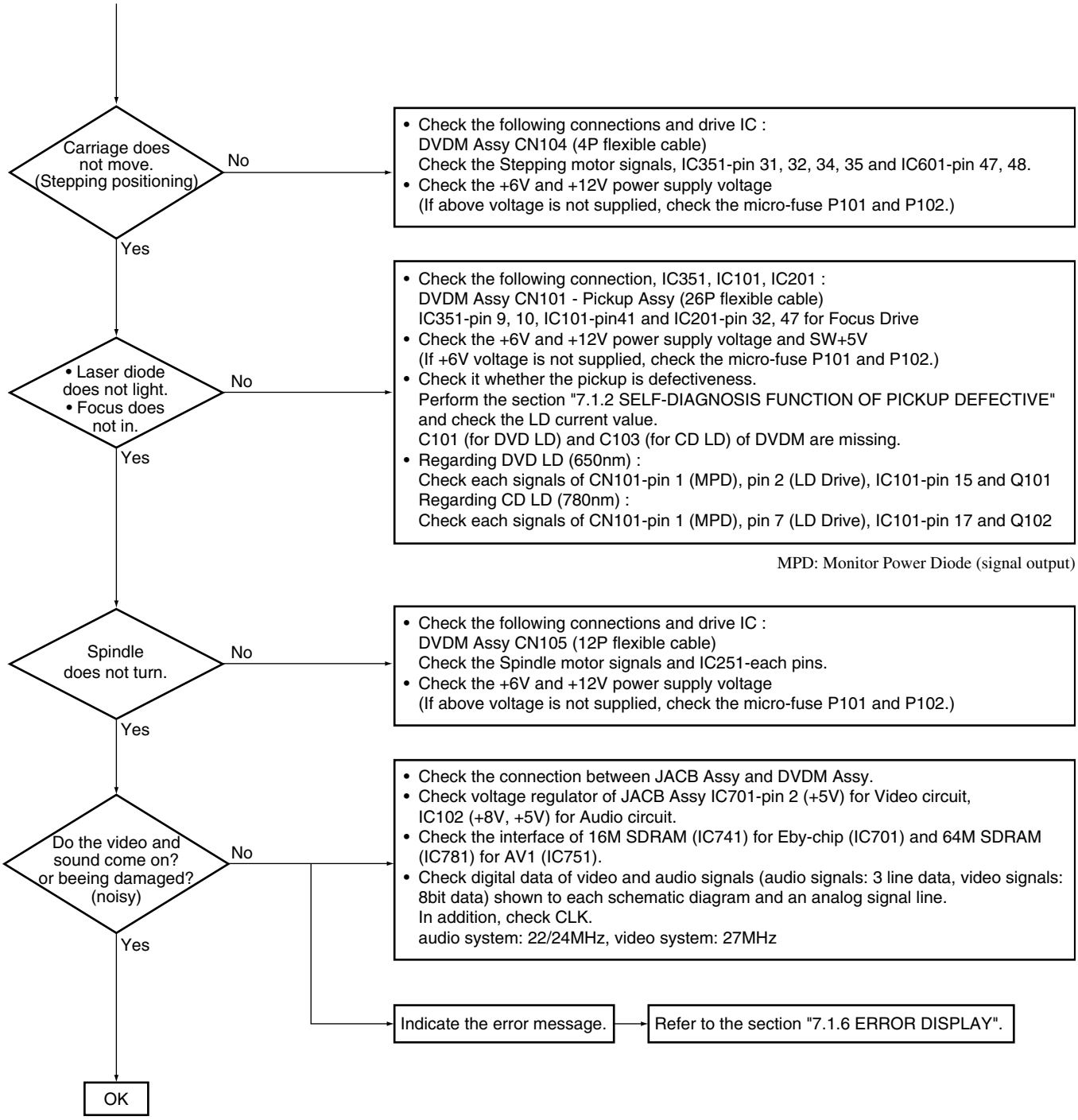


(18) Foot of R959 (Y)
V: 0.2V/div. H: 10µsec/div.



7.1.8 TROUBLE SHOOTING




Carriage does not move. (Stepping positioning)
No
Yes
• Check the following connections and drive IC :
DVDM Assy CN104 (4P flexible cable)
Check the Stepping motor signals, IC351-pin 31, 32, 34, 35 and IC601-pin 47, 48.
• Check the +6V and +12V power supply voltage
(If above voltage is not supplied, check the micro-fuse P101 and P102.)
• Laser diode does not light.
• Focus does not in.
No
Yes
• Check the following connection, IC351, IC101, IC201 :
DVDM Assy CN101 - Pickup Assy (26P flexible cable)
IC351-pin 9, 10, IC101-pin41 and IC201-pin 32, 47 for Focus Drive
• Check the +6V and +12V power supply voltage and SW+5V
(If +6V voltage is not supplied, check the micro-fuse P101 and P102.)
• Check it whether the pickup is defectiveness.
Perform the section "7.1.2 SELF-DIAGNOSIS FUNCTION OF PICKUP DEFECTIVE" and check the LD current value.
C101 (for DVD LD) and C103 (for CD LD) of DVDM are missing.
• Regarding DVD LD (650nm) :
Check each signals of CN101-pin 1 (MPD), pin 2 (LD Drive), IC101-pin 15 and Q101
Regarding CD LD (780nm) :
Check each signals of CN101-pin 1 (MPD), pin 7 (LD Drive), IC101-pin 17 and Q102
MPD: Monitor Power Diode (signal output)
Spindle does not turn.
No
Yes
• Check the following connections and drive IC :
DVDM Assy CN105 (12P flexible cable)
Check the Spindle motor signals and IC251-each pins.
• Check the +6V and +12V power supply voltage
(If above voltage is not supplied, check the micro-fuse P101 and P102.)
Do the video and sound come on? or beeing damaged? (noisy)
No
Yes
• Check the connection between JACB Assy and DVDM Assy.
• Check voltage regulator of JACB Assy IC701-pin 2 (+5V) for Video circuit, IC102 (+8V, +5V) for Audio circuit.
• Check the interface of 16M SDRAM (IC741) for Eby-chip (IC701) and 64M SDRAM (IC781) for AV1 (IC751).
• Check digital data of video and audio signals (audio signals: 3 line data, video signals: 8bit data) shown to each schematic diagram and an analog signal line.
In addition, check CLK.
audio system: 22/24MHz, video system: 27MHz
Indicate the error message.
Refer to the section "7.1.6 ERROR DISPLAY".
OK

7.1.9 DISASSEMBLY

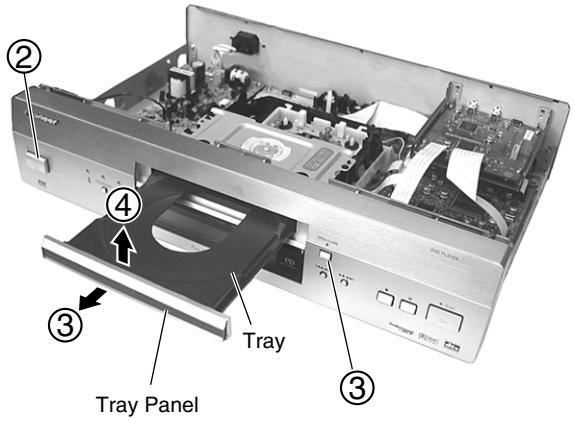
■ DIAGNOSIS OF PCBs

Note :

When diagnosing the unit, be sure to use two Extension Cables for service (Part No. : GGF1157, GGD1298) and a Extension Board for service (Part No. : GGF1430).

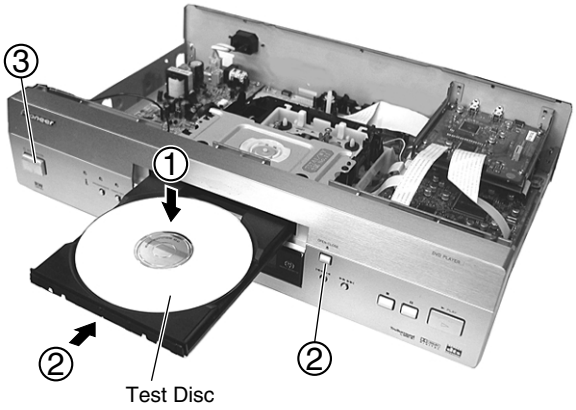
1 Bonnet and Tray Panel

① Remove the Bonnet (Screws × 5).
② Turn power ON.
③ Open the Tray (⏏).
④ Remove the Tray Panel.



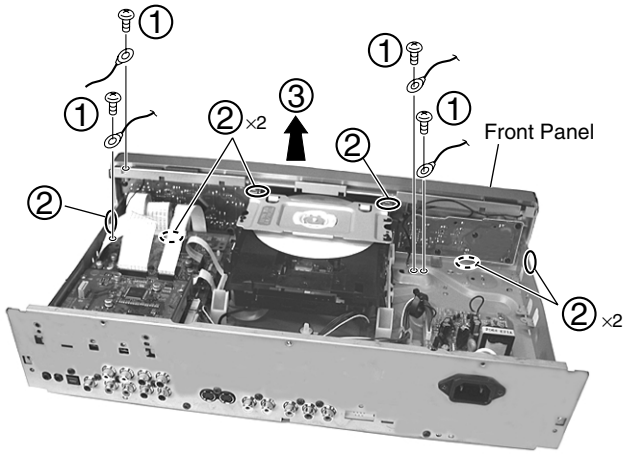
2 Test Disc Set

① Set the Test Disc.
② Close the Tray (⏏). → Clamp the Test Disc.
③ Turn power OFF.
④ Pull out the Power Cord from the outlet.



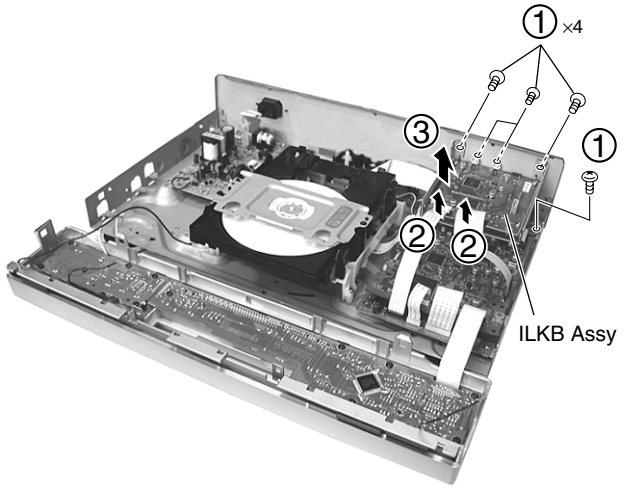
3 Front Panel

① Remove four Earth Lead Unit (Screws × 4).
② Unhook (× 6).
③ Remove the Front Panel.



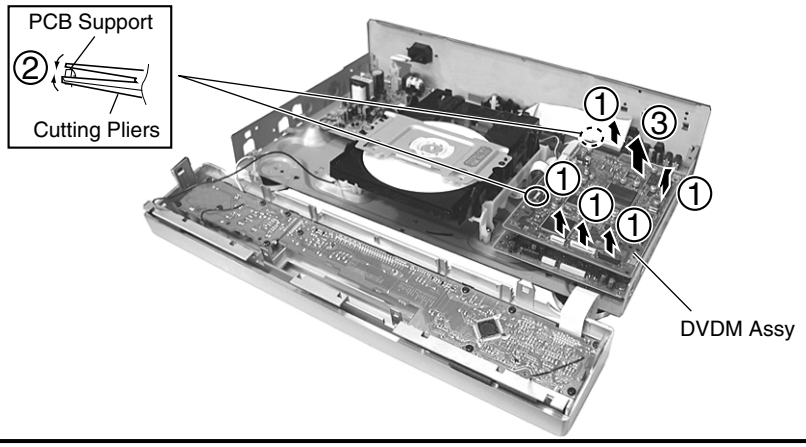
4 ILKB Assy

① Remove five screws.
② Release two Flexible Cables.
③ Remove the ILKB Assy.



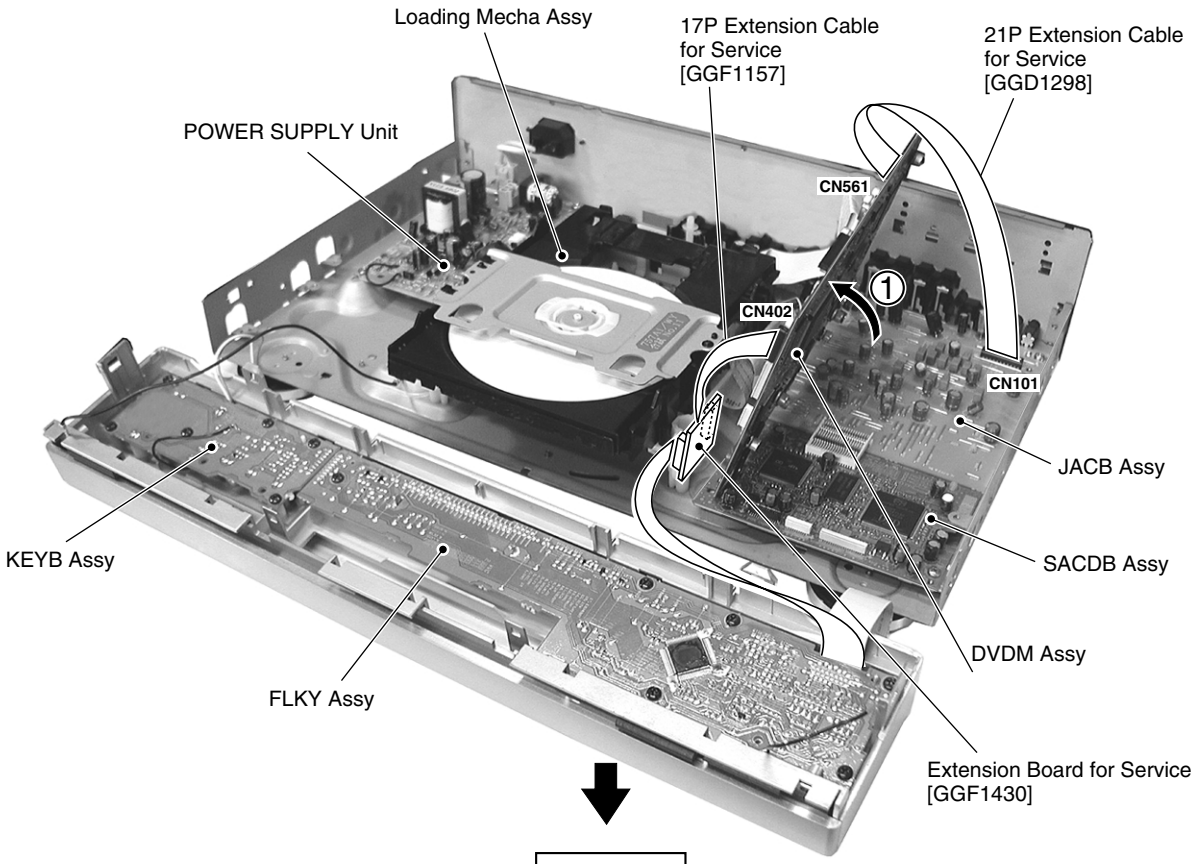
5 DVDM Assy

① Release five Flexible Cables.
② Release from two PCB Supports.
③ Remove the DVDM Assy.



6 Diagnosis

① Stand the DVDM Assy as figure below.
② Connect two Extension Cables for Service and a Extension Board for Service as figure below.



Diagnosis

Connection Diagram of Housing Assy

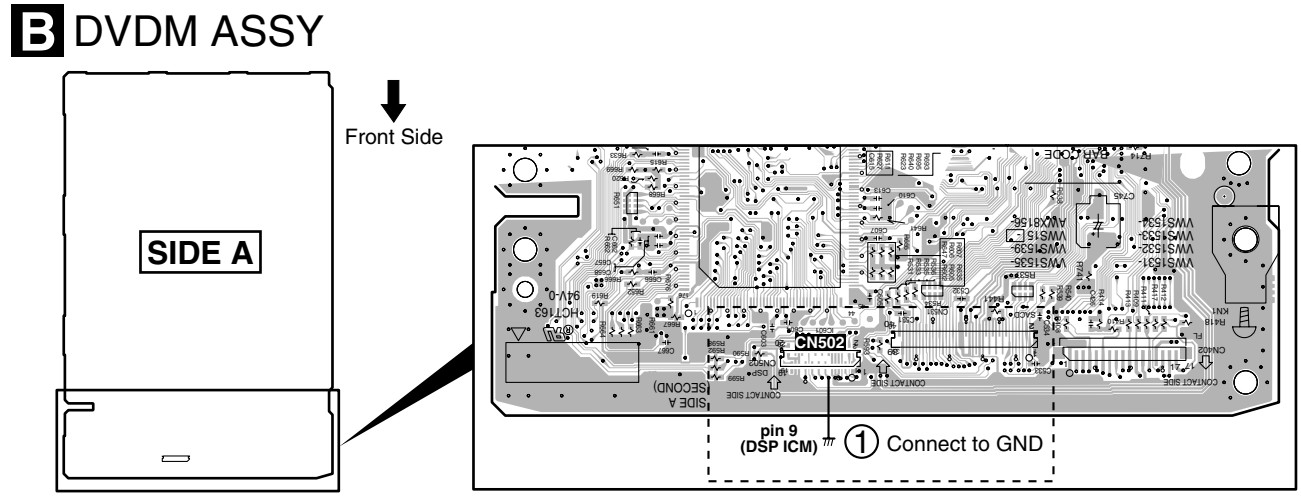
At the time of re-assembly, connect each wire rod justly.
AC Inlet Assy → CN1
Housing Assy → CN2

☞Diagnosis Method of Audio Block

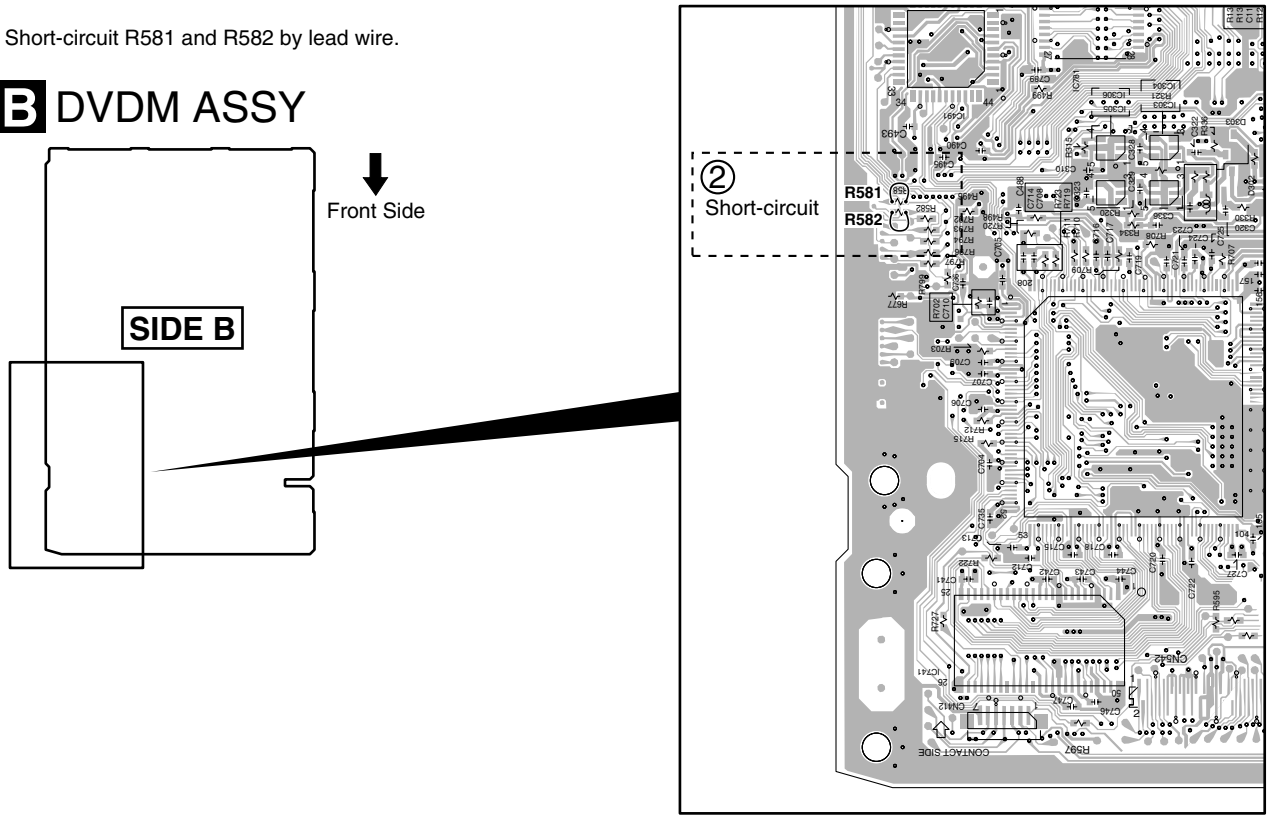
● How to diagnose each audio signal of DVDM Assy without installing the SACDB Assy

[Do not connectes between CN502 (DVDM) ↔ CN801 (SACDB) , CN531 (DVDM) ↔ CN901 (SACDB) of FFCs.]

① Connect pin 9 of CN502 (DSP ICM) on the DVDM Assy to GND.



② Short-circuit R581 and R582 by lead wire.



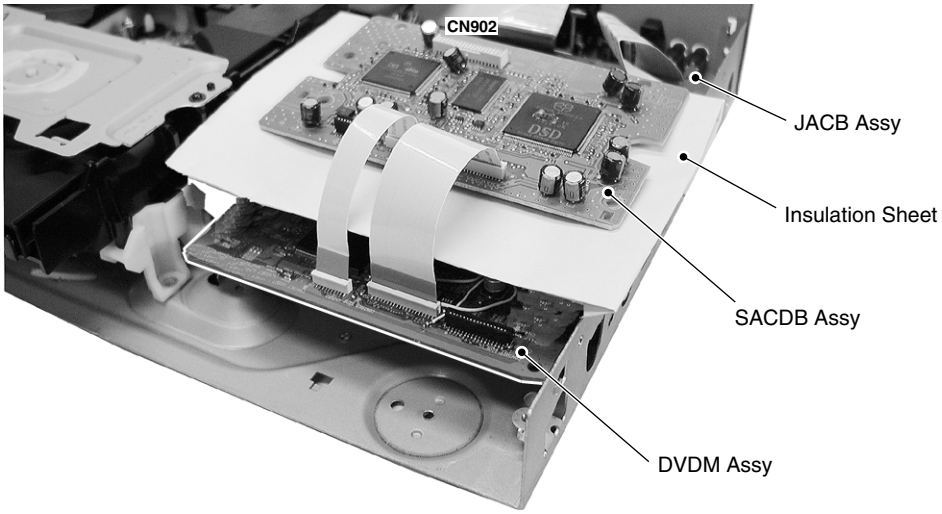
③ To confirm the Front L/R ch,
set "**Audio Output Mode**" of "**Speakers**" in "**The Initial Settings Menu**" to "**2 channel**", and playback the disc.

④ To confirm the Surround Ls/Rs ch and Center/Subwoofer ch,
turn the above setting into "**5.1 channel**", and playback the disc (Ls/Rs and Center/Subwoofer signals are recorded).

● How to diagnose the SACD and DSP blocks of the SACDB Assy

① Remove a Board to Board connector CN102 (JACB) ↔ CN902 (SACDB) .

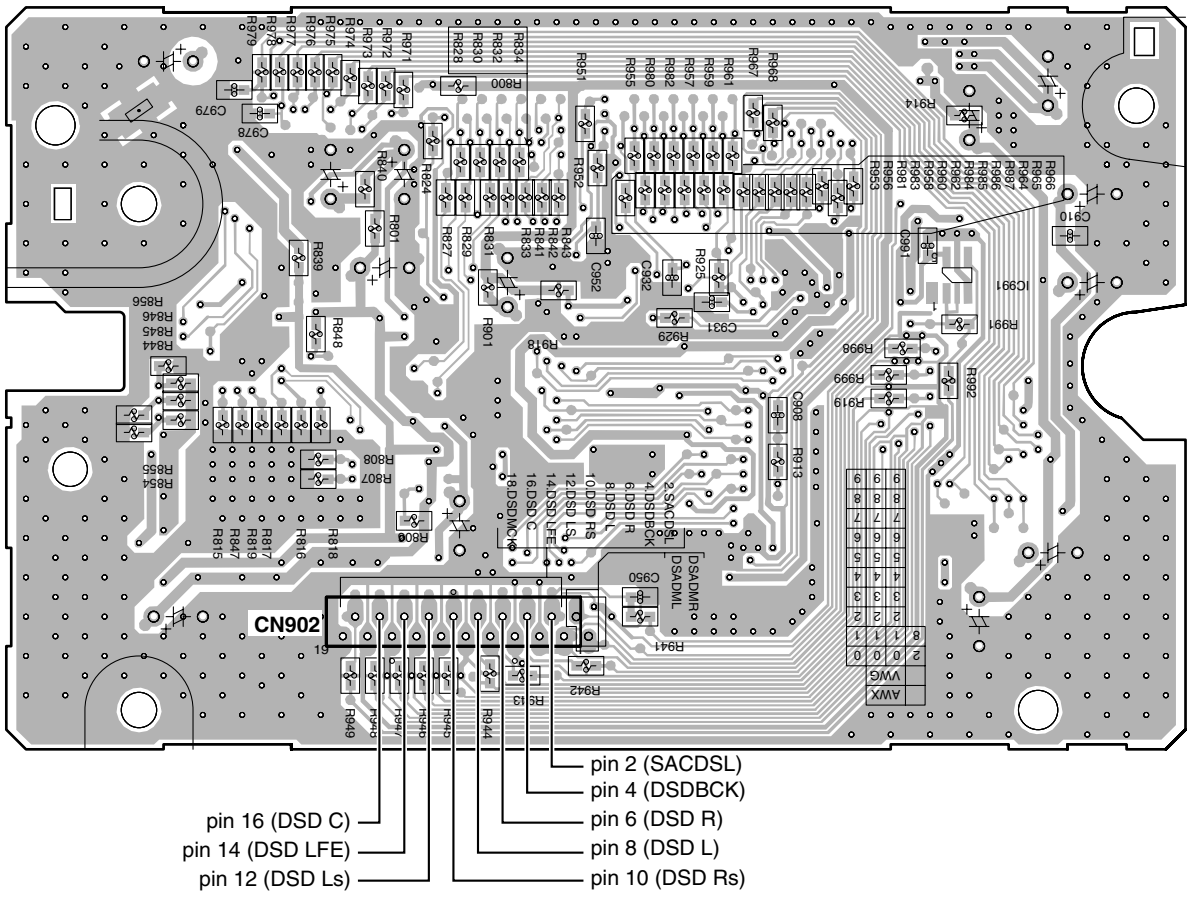
② styling like figure below.



③ In this case an audio of SACD is not output from the Audio jack.
However, observe the signal waveform of CN902 on the SACDB Assy, and can confirm it.
CN902 - pin 2 (SACDSL), pin 4 (DSDBCK), pin 6 (DSD R), pin 8 (DSD L),
pin 10 (DSD Rs), pin 12 (DSD Ls), pin 14 (DSD LFE), pin 16 (DSD C).

D SACDB ASSY

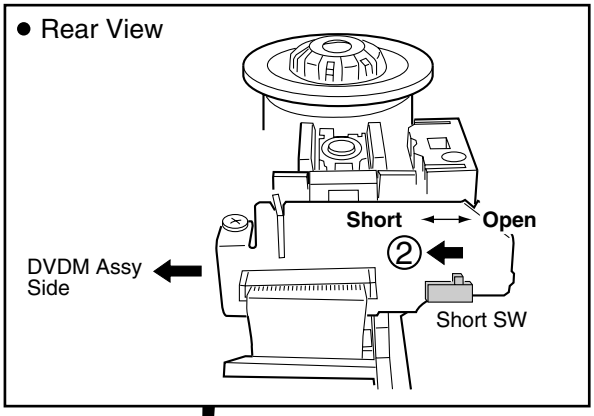
SIDE B

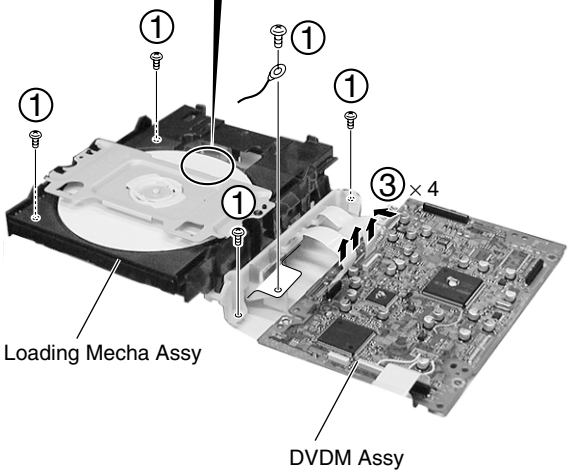


Disassembly of the Traverse Mechanism Assy and the Pickup Assy

1 Loading Mecha Assy

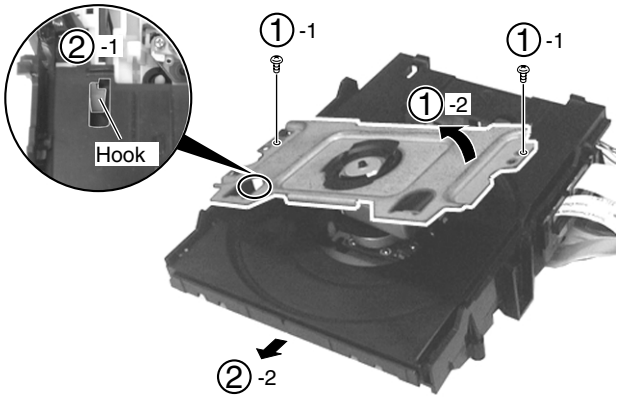
① Remove five Screws.
② Turn the Short SW to short side.
③ Remove three Flexible Cables and a Connector.





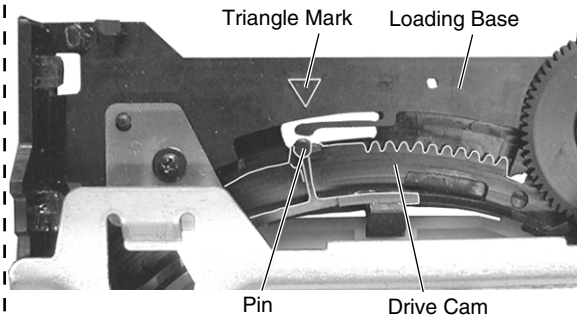
2 Tray

① Remove the Bridge (Screw ×2).
② Pull out the Tray and remove it while unhooking a hook.



☞Caution in the Tray Insertion

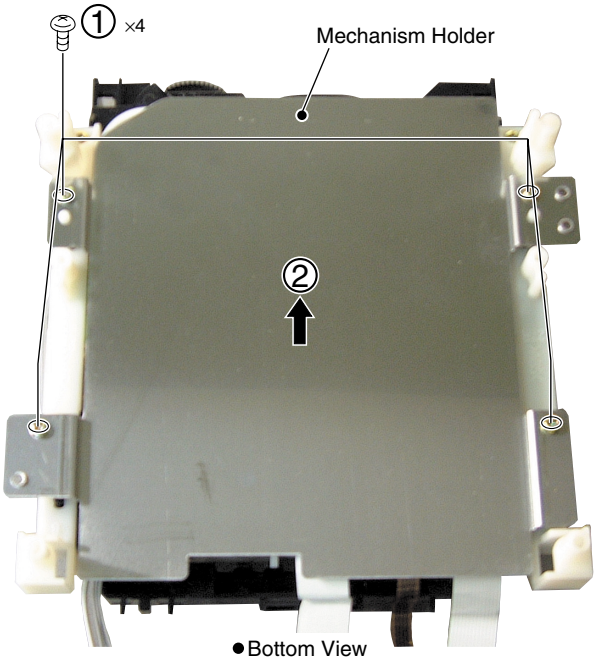
In the Tray insertion, insert it after matching a triangle mark of the Loading Base and a position of pin of the Drive Cam.



3 Traverse Mechanism Assy-S and Pickup Assy-S

① Remove four screws.

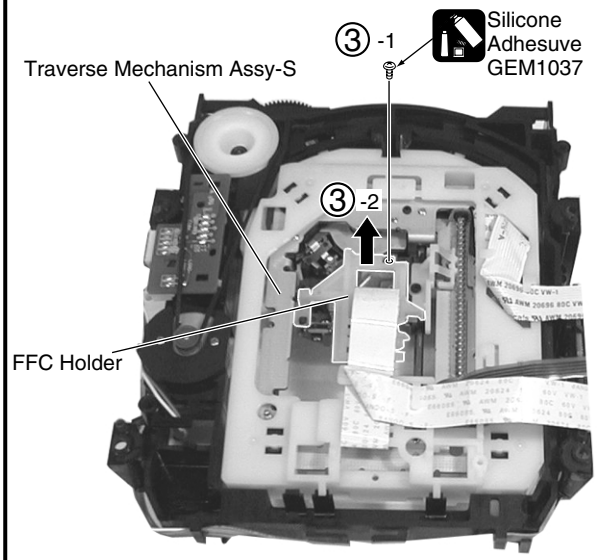
② Remove the Mechanism Holder.



● Bottom View

③ Remove the FFC Holder with the state which Flexible Cable was atatched. (Screw × 1)

Cautions :
Screw is locked with Silicone Adhesive.
Please lock it with Silicone Adhesive when installs it.



● Bottom View

Traverse Mechanism Assy

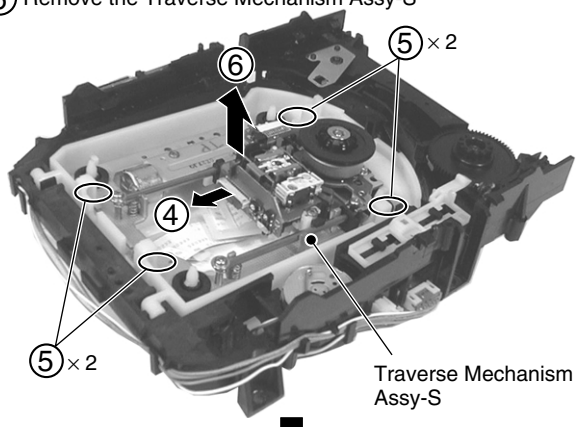
Pickup Assy

● When Removing The Traverse Mechanism Assy

④ Remove the Pickup Flexible Cable

⑤ Unhook (×4)

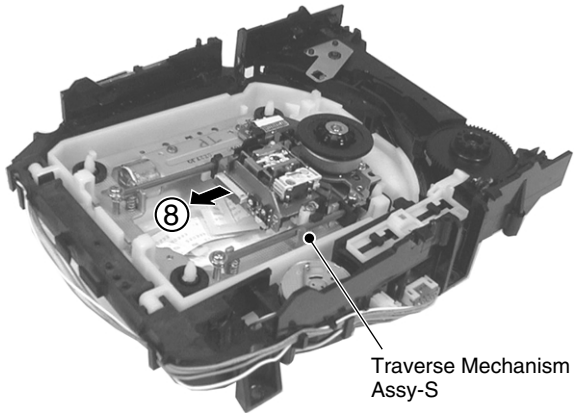
⑥ Remove the Traverse Mechanism Assy-S



Exchange

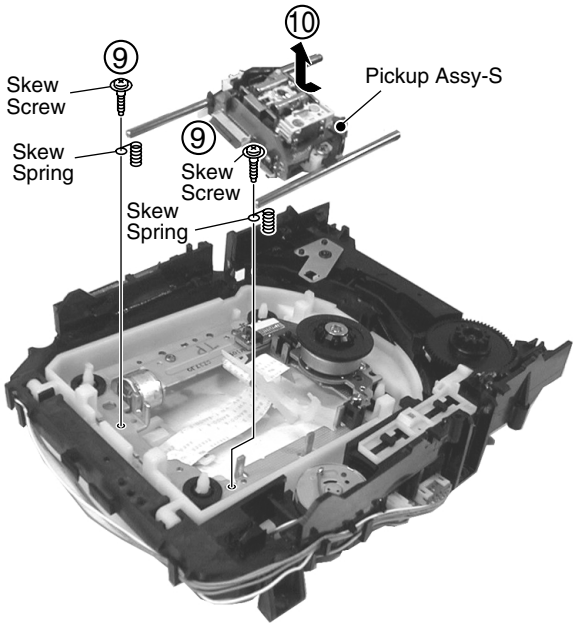
● When Removing The Pickup Assy

⑦ Remove the Pickup Flexible Cable.



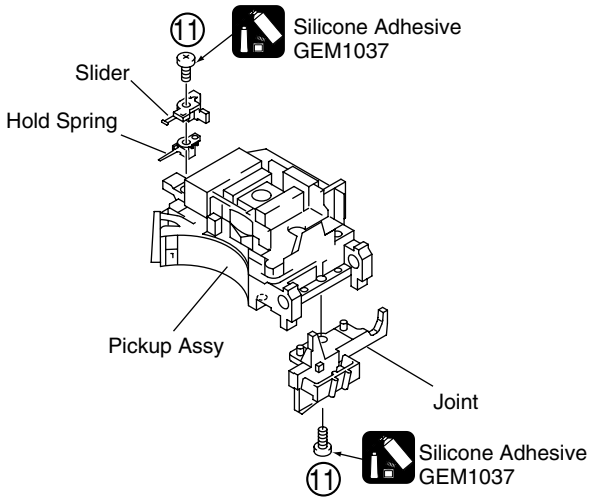
⑨ Remove two Skew Screws and two Skew Springs.

⑩ Remove the Pickup Assy-S.



⑪ Remove two screws.

Cautions:
Screw is locked with Silicone adhesive.
Please lock it with Silicone adhesive when installs it.

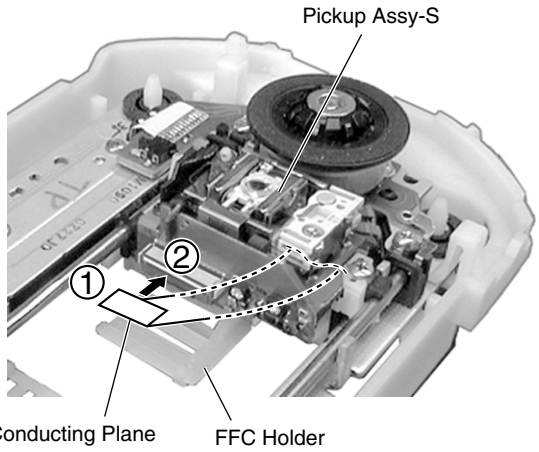


Exchange

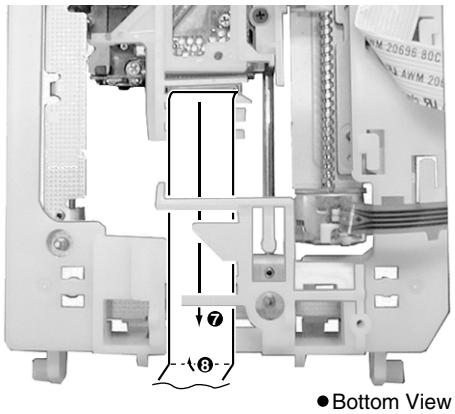
☞STYLING THE PICKUP FLEXIBLE CABLE

① FOLD a edge of lining part of the Pickup Flexible Cable.

② Insert the Pickup Flexible Cable in connector, and lock it surely.

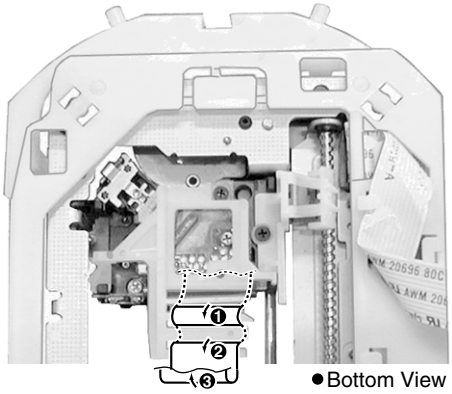


Caution :
Move the Pickup to the innermost of the disc

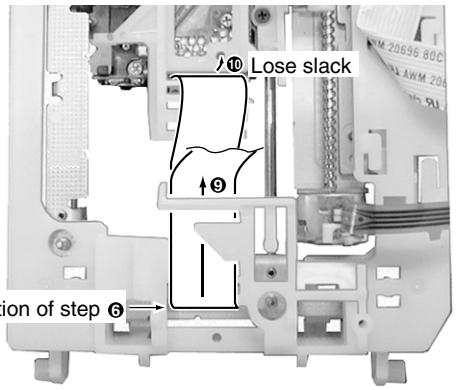


● Bottom View

③ Perform the styling as shown in figure below.

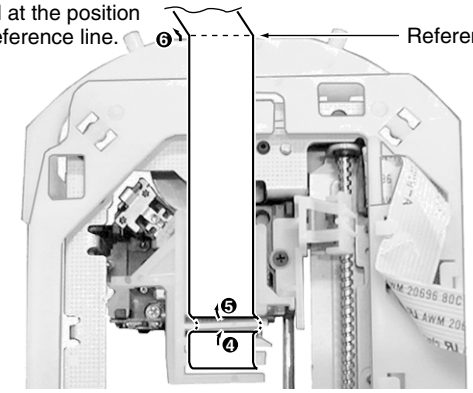


● Bottom View

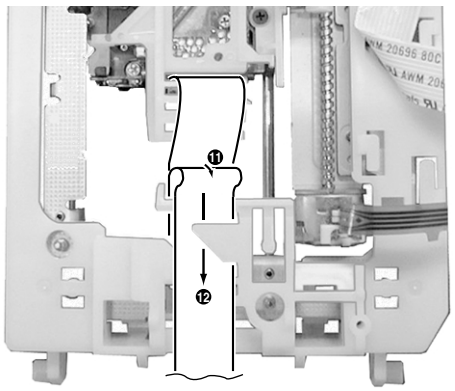


● Bottom View

Fold at the position of reference line. ❻ ← Reference line



● Bottom View



● Bottom View

7.2 IC

• The information shown in the list is basic information and may not correspond exactly to that shown in the schematic diagrams.

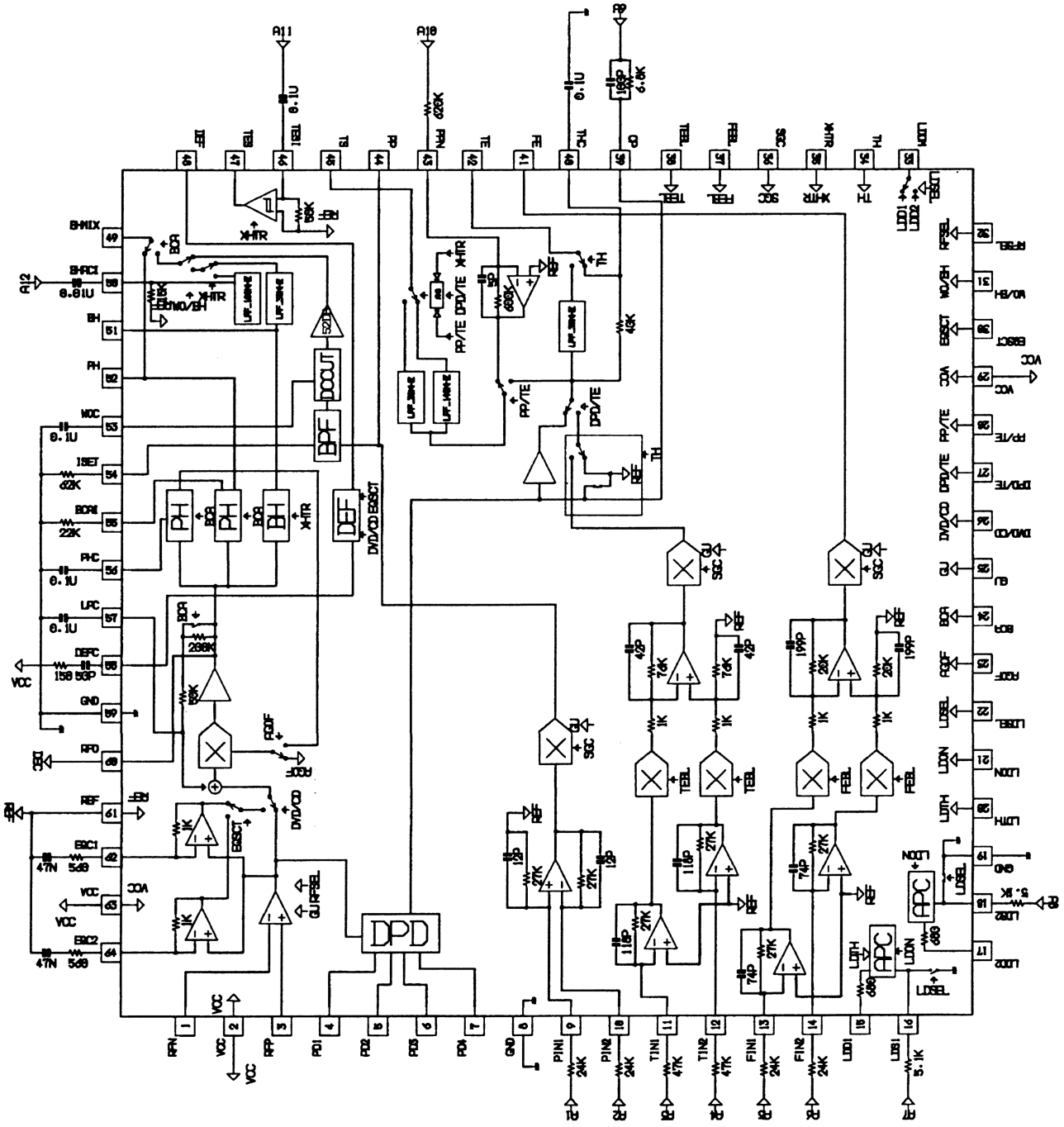
• List of IC

LA9704W, LC78652W, BA6664FM, SM8707HV, PD6345A, M65776AFP, PCM1738EG-3, DSD1702EG, LA73054, CXD2753R, PE5314B, PE5286A, PD0274A, ADV7300AKST, PM0033A, TSB43CA43GGW, PD5787A

■ LA9704W (DVDM ASSY : IC101)

• RF IC

● Block Diagram



● Pin Function

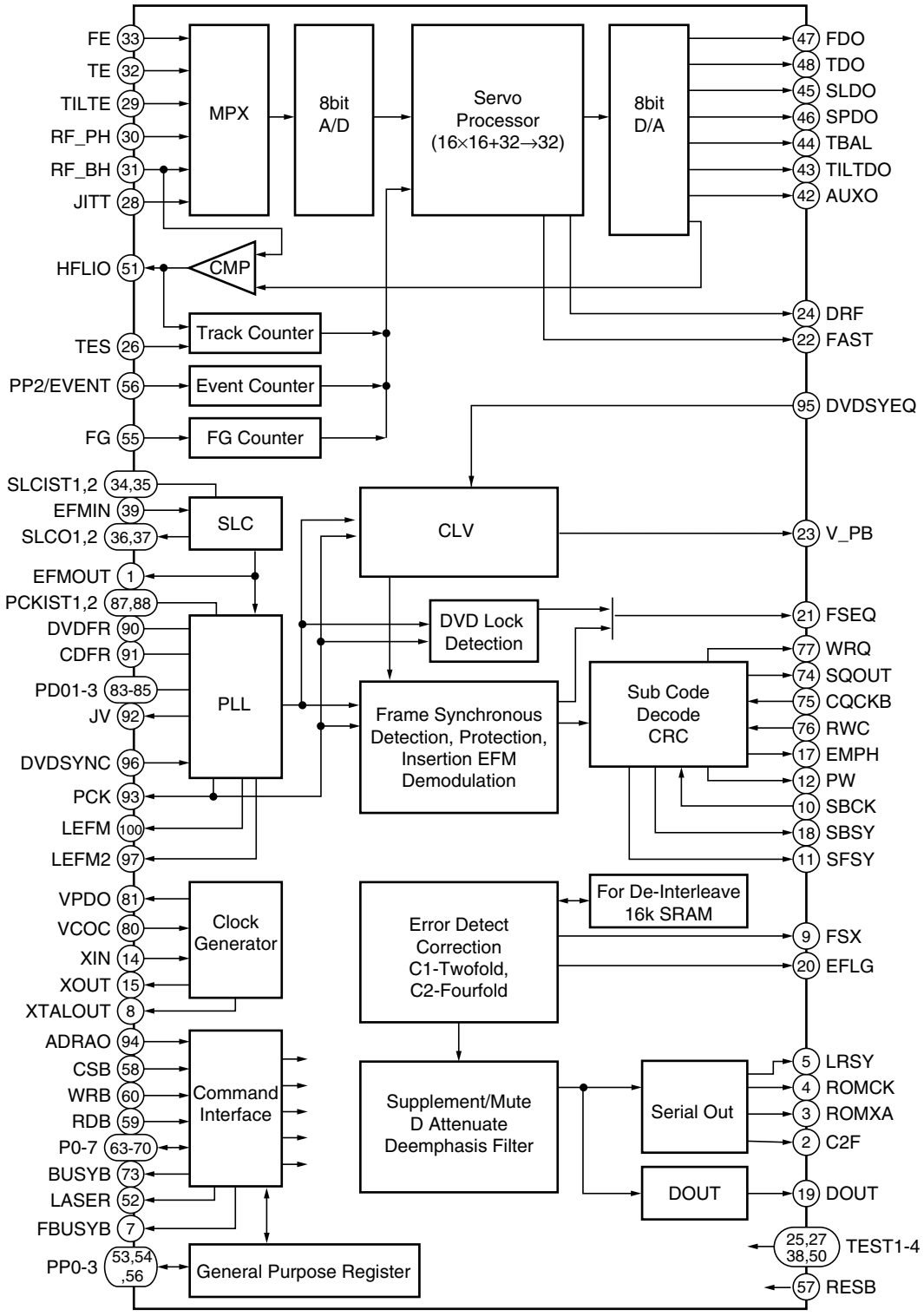
No.	Pin name	Pin Functions
1	RFN	RF- input
2	VCC	Power supply terminal (for DPD)
3	RFP	RF+ nput
4	PD1	Pickup signal input
5	PD2	
6	PD3	
7	PD4	
8	GND	Ground (for DPD)
9	PIN1	Pickup signal input
10	PIN2	
11	TIN1	
12	TIN2	
13	FIN1	
14	FIN2	
15	LDD1	APC1 output
16	LDS1	APC1 monitor input
17	LDD2	APC2 output
18	LDS2	APC2 monitor input
19	GND	Ground (Servo system)
20	LDTH	APC1 threshold change (H: VCC-1.5V, L: 180mV)
21	LDON	Laser ON terminal (H: ON)
22	LDSEL	APC change terminal (H: APC1)
23	AGOF	RFAGC off terminal
24	BCA	PH electric discharge coefficient change (H: BCA mode)
25	GU	RF, Servo signal gain up terminal (H: Gain up)
26	DVD/CD	RF- equalizer band change terminal (H: DVD)
27	DPD/TE	TE output change terminal (H: DPD)
28	PP/TE	TS output change terminal (H: PP)
29	VCC	Power supply terminal (Servo system)
30	EQSCT	EQ change for CD (H: 62 pin choice)
31	WO/BH	BHMIX output change terminal (H: WOBLE)
32	RFSEL	RF amplifier gain change (H: 6dB up)
33	LDDM	LDD monitor terminal
34	TH	Tracking hold (H: hold)
35	XHTR	Tracking, Bottom band change (L: High bandwidth)
36	SGC	Servo gain control terminal (FE, PP, TE)
37	FEBL	FE balance adjustment terminal
38	TEBL	TE balance adjustment terminal
39	CP	Resistance for charge pump gain setting, a condenser connection terminal
40	THC	Volume connection terminal for tracking hold
41	FE	Focus error output
42	TE	Tracking error output
43	PPN	Ohms connection terminal for push-pull gain setting
44	PP	Push-pull output terminal

No.	Pin name	Pin Functions
45	TS	Tracking cross signal output
46	TESI	TES comparator input terminal
47	TES	TES output
48	DEF	Deffect search
49	BHMIX	PH, BH, woble change output
50	BHACI	BH– AC input
51	BH	RF bottom detection output
52	PH	RF peak detection output
53	WOC	Volume connection terminal for DC cut
54	ISET	Ohms connection terminal for BPF center frequency setting
55	BCAI	Ohms connection terminal for peak hold detection fixed number setting (In BCA)
56	PHC	PH detection condenser connection terminal for RF-AGC
57	LPC	Condenser connection terminal for RF DC servo
58	DEFC	Volume connection terminal for deffect search
59	GND	Ground (RF system)
60	RFO	RF output terminal
61	REF	Reference output terminal
62	EQC1	Equalizer setting terminal for CD
63	VCC	Power supply terminal (RF system)
64	EQC2	Equalizer setting terminal for CD

■ LC78652W (DVDM ASSY : IC201)

• Servo DSP IC

● Block Diagram



● Pin Function

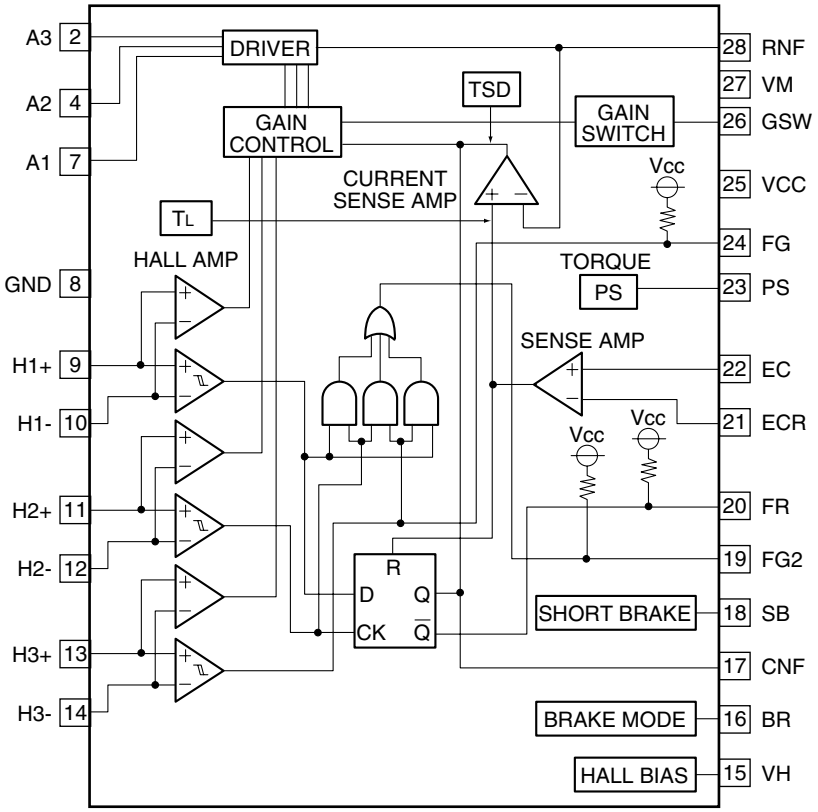
No.	Pin Name	I/O	Pin Function
1	EFMOUT	O	Output the state that was binary-stated value EFM
2	C2F	O	C2 flag output
3	ROMXA	O	CD-ROM data output
4	ROMCK	O	Shift clock output for CD-ROM data output
5	LRSY	O	L/R clock output for CD-ROM data output
6	PP3	I/O	General-purpose port input/output / DVD sync. signal input N ch-OD output
7	FBUSYB	O	Busy signal output of DSP process operation N ch-OD output
8	XTALOUT	O	External system clock output
9	FSX	O	CD 1 frame sync. signal output
10	SBCK	I	Subcode reading out clock input
11	SFSY	O	Frame sync. signal output of subcode
12	PW	O	Subcode P, Q, R, S, T, U, V and W output
13	VSS	–	GND pin
14	XIN	I	Connect a crystal resonator (16.9344MHz)
15	XOUT	O	Connect a crystal resonator
16	DVDD1	–	3.3V power supply of the oscillation circuit
17	EMPH	O	Monitor pin of the deemphasis
18	SBSY	O	Sync. signal output of the subcode block
19	DOUT	O	Audio EIAJ data output
20	EFLG	O	Error correction state monitor of the error correction C1 and C2
21	FSEQ	O	Detection monitor of the CD/DVD frame sync. signal
22	FAST	O	Playback speed monitor N ch-OD output
23	V_PB	O	Monitor output of the rough servo/CLV control
24	DRF	O	In focus monitor
25	TEST3	I	Test input 3
26	TES	I	Tracking error signal input
27	TEST2	I	Test input 2
28	JITT	I	Jitter quantity detecting signal input of EFM PLL
29	TILTE	I	Tilt error signal input
30	RF_PH	I	RF peak hold signal input
31	RF_BH	I	RF bottom hold signal input
32	TE	I	Tracking error signal input
33	FE	I	Focus error signal input
34	SLCIST1	–	Current setting pin 1 of the constant current charge pump for SLC
35	SLCIST2	–	Current setting pin 2 of the constant current charge pump for SLC
36	SLCO1	O	Control output 1 for SLC
37	SLCO2	O	Control output 2 for SLC
38	TEST1	I	Test input 1
39	EFMIN	I	EFM/EFM + input
40	AVDD	–	5V power supply of A/D and D/A for servo
41	AVSS	–	GND of A/D and D/A for servo
42	AUXO	O	DA auxiliary output
43	TILTDO	O	Tilt control signal output
44	TBAL	O	Tracking balance control signal output
45	SLDO	O	Sled control signal output
46	SPDO	O	Spindle control signal output
47	FDO	O	Focus control signal output
48	TDO	O	Tracking control signal output
49	VREF	–	Reference level of D/A for servo
50	TEST4	I	Test input 4

No.	Pin Name	I/O	Pin Function
51	HFLIO	I/O	Mirror detection signal input/output
52	LASER	O	Output pin for laser ON/OFF control
53	PP0/DVD_CDB	I/O	General-purpose port input/output / Disc discrimination signal output
54	PP1/CRCERRB	I/O	General-purpose port input/output / Subcode CRC result signal output
55	FG	I	FG counter input
56	PP2/EVENT	I/O	General-purpose port input/output / Event counter input
57	RESB	I	Reset input
58	CSB	I	Chip select input
59	RDB	I	Internal state reading signal input
60	WRB	I	Command / data writing signal input
61	DVDD2	–	5V power supply
62	VSS	–	GND
63	P0	I/O	Command / data input/output
64	P1		
65	P2		
66	P3		
67	P4		
68	P5		
69	P6		
70	P7		
71	VSS	–	GND
72	DVDD1	–	3.3V power supply for internal
73	BUSYB	O	Busy signal output of command process
74	SQOUT	O	Serial output of subcode Q
75	CQCKB	I	Shift clock input for subcode Q data output
76	RWC	I	Update permission input of subcode Q
77	WRQ	O	Read out ready monitor of subcode Q
78	AVSS	–	PLL GND for internal system clock
79	VRPFR	–	VCO oscillation range setting of PLL for system clock
80	VCOC	I	Connect a PLL filter for system clock
81	VPDO	O	
82	AVDD	–	PLL 5V power supply for system clock
83	PDO1	I/O	PLL filter connection pin 1 for EFM playback
84	PDO2	I/O	PLL filter connection pin 2 for EFM playback
85	PDO3	I/O	PLL filter connection pin 3 for EFM playback
86	AVSS	–	PLL GND for EFM playback
87	PCKIST1	–	Current setting 1 of PLL constant current charge pump for EFM playback
88	PCKIST2	–	Current setting 2 of PLL constant current charge pump for EFM playback
89	AVDD	–	PLL 5V power supply for EFM playback
90	DVDFR	–	VCO oscillation range setting of PLL for EFM playback 1
91	CDFR	–	VCO oscillation range setting of PLL for EFM playback 2
92	JV	O	Jitter output of PLL clock for EFM playback
93	PCK	O	Bit clock output for EFM playback
94	ADRAO	I	Address input
95	DVDSYEQ	I	DVD synchronize pulse input
96	DVDSYNC	I	DVD synchronous signal input
97	LEFM2	O	Output the state that cut and out a signal which was binary-stated value EFM with PCK 2
98	DVDD1	–	3.3V power supply for I/O
99	VSS	–	GND
100	LEFM	O	Output the state that cut and out a signal which was binary-stated value EFM with PCK 1

■ BA6664FM (DVDM ASSY : IC251)

• Three-phase Motor Driver

● Block Diagram



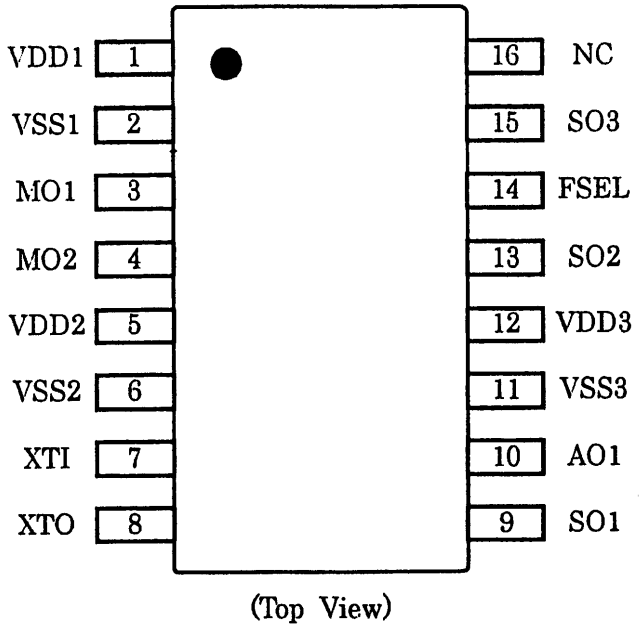
● Pin Function

No.	Pin Name	Pin Function	No.	Pin Name	Pin Function
1	N.C.	N.C.	16	BR	Brake mode switching pin
2	A3	Output pin	17	CNF	Capacitor connection pin for phase compensation
3	N.C.	N.C.	18	SB	Short brake pin
4	A2	Output pin	19	FG2	FG 3-phase mix signal output pin
5	N.C.	N.C.	20	FR	Rotation detecting pin
6	N.C.	N.C.	21	ECR	Control reference pin of output voltage
7	A1	Output pin	22	EC	Output voltage control pin
8	GND	GND pin	23	PS	Power save pin
9	H1+	Hall signal input pins	24	FG	FG signal output pin
10	H1-		25	VCC	Power supply pin
11	H2+		26	GSW	Gain switching pin
12	H2-		27	VM	Motor power pin
13	H3+		28	RNF	Resistor connection pin for output current detection
14	H3-		FIN	FIN	GND
15	VH	Hall bias pin			

■ SM8707HV (DVDM ASSY : IC481)

• Clock Generate IC

● Pin Arrangement



(Top View)

● Pin Function

No.	Pin name	Dir.	Pin Functions
1	VDD1	PWR	Power supply terminal 1 (digital business)
2	VSS1	GND	Earth terminal 1 (digital business)
3	MO1	OUT	Video output terminal 1 (the 27MHz fixed output)
4	MO2	OUT	Video output terminal 2 (the 27MHz fixed output)
5	VDD2	PWR	Power supply terminal 2 (analog business)
6	VSS2	GND	Earth terminal 2 (analog business)
7	XTI	IN	External clock input terminal or crystal resonator connection
8	XTO	OUT	Crystal resonator connection terminal
9	SO1	OUT	Signal conditioning system output terminal 1 (36.8640MHz fixation)
10	AO1	OUT	Sound output terminal 1 (the 512fs output)
11	VSS3	GND	Earth terminal 3 (digital business)
12	VDD3	PWR	Power supply terminal 3 (digital business)
13	SO2	OUT	Signal conditioning system output terminal 2 (16.9344MHz fixation)
14	FSEL	IN	Sampling frequency change terminal FSEL= "L": fs=48kHz FSEL= "H": fs=44.1kHz (There is inside pull-up resister, Schmidt trigger input)
15	SO3	OUT	Signal conditioning system output terminal 3 (33.8688MHz fixation)
16	NC	–	Unused terminal

■ PD6345A (DVDM ASSY : IC601)

• FR CPU

● Pin Function

No.	Mark	Pin Name	I/O	Pin Function
1	P20/D16	D0	I/O	Data bus input/output
2	P21/D17	D1		
3	P22/D18	D2		
4	P23/D19	D3		
5	P24/D20	D4		
6	P25/D21	D5		
7	P26/D22	D6		
8	P27/D23	D7		
9	P30/D24	D8		
10	P31/D25	D9		
11	P32/D26	D10		
12	P33/D27	D11		
13	P34/D28	D12		
14	P35/D29	D13		
15	P36/D30	D14		
16	P37/D31	D15		
17	VSS	GND	–	Ground
18	P40/A00	A0	O	Address bus output
19	P41/A01	A1		
20	P42/A02	A2		
21	P43/A03	A3		
22	P44/A04	A4		
23	P45/A05	A5		
24	P46/A06	A6		
25	P47/A07	A7		
26	VCC3	V+3.3D	–	Power supply
27	VCC2	V+2.5D	–	Power supply
28	P50/A08	A8	O	Address bus output
29	P51/A09	A9		
30	P52/A10	A10		
31	P53/A11	A11		
32	P54/A12	A12		
33	P55/A13	A13		
34	P56/A14	A14		
35	P57/A15	A15		
36	VSS	GND	–	Ground
37	P60/A16	A16	O	Address bus output
38	P61/A17	A17		
39	P62/A18	A18		
40	P63/A19	A19		
41	P64/A20	A20		
42	P65/A21	A21		
43	P66/A22	A22		
44	P67/A23	WBL	O	For Wobble detection corresponding to DVD R/W (main)
45	DAVS	GND	–	Ground
46	DAVC	V+3.3D	–	Power supply
47	DA0	STEP1	I	For stepping motor control
48	DA1	STEP2	I	
49	DA2	LODRV	I	Loading, door and select motor drive

No.	Mark	Pin Name	I/O	Pin Function
50	AN0	NC	I	NC
51	AN1	NC	I	NC
52	AN2	NC	I	NC
53	AN3	XOEM	I	OEM model protection input
54	AN4	LDREAD	I	Input for LD current value indication
55	AN5	NC	I	NC
56	AN6	NC	I	NC
57	AN7	LODPOS	I	Loading clamp position SW input
58	AVCC	V+3.3D	–	Power supply
59	AVRH	V+3.3D	–	Power supply
60	AVSS/AVRI	GND	–	Ground
61	VSS	GND	–	Ground
62	PP0/ATGX	SLDPOS	I	SW input of slider inside position
63	PP1/FRCK	GSW	O	Gain up at ACBR (at ACBR: H, others: L)
64	PP2/IN0	780ON	I	ON/OFF control signal of 780nm laser diode
65	PP3/IN1	GU	O	RF, servo signal gain up terminal (H: Gain up)
66	PP4/IN2	XMON	O	Mute of DRV (spindle motor ON: H)
67	PP5/IN3	XDRVMUT	O	FTS driver mute output
68	PP6	LT1_3V	O	Communication response to the FL controller
69	PP7	XRDY_3V	I	Communication request from the FL controller
70	VCC3	V+3.3D	–	Power supply
71	VCC2	V+2.5D	–	Power supply
72	PO0/OC0	XCURDET	I	Actuator current detection input Servo OFF for "L" 300ms
73	PO1/OC1	XCBUSY	I	Busy signal of command process Command acceptable : "L"
74	PO2/OC2	XDSPRST	O	Servo DSP reset
75	PO3/OC3	BCA	–	BCA read signal (at BCA read: H) (Not used)
76	PO4/OC4	NC	I	NC
77	PO5/OC5	PPCNT	O	Switch of TZC in WBL traversal (at PP: H)
78	PO6/OC6	XDFINH	O	Defect signal control (DEFECT ON: Hi-Z; OFF: "L")
79	PO7/OC7	DPD/TE	O	H=1 beam, L=3 beams
80	VSS	GND	–	Ground
81	PN0/AIN0	DVD/XCD	O	RF EQ switching signal at DVD/CD "H": DVD, "L": CD
82	PN1/BIN0	AGOFF	O	"H": Turn off AGC of RFIC
83	PN2/AIN1	650X780	O	780nm/650nm switching signal
84	PN3/BIN1	LD ON	O	ON/OFF control signal of laser diode
85	PN4/AIN2	WBLSEL	O	NC
86	PN5/BIN2	RFSEL	O	RF amplifier gain change terminal (H: Gain up)
87	PN6/AIN3	XCD2X	O	For VCD double speed playback
88	PN7/BIN3	OEICG	O	"H": Gain of OEIC up to 6dB
89	PM0/ZIN0	EN33M	O	NC
90	PM1/ZIN1	EN24M	O	NC
91	PM2/ZIN2	V SEL	O	(Composite, S) / (YCbCr) or (RGB) switch
92	PM3/ZIN3	V SEL2	O	(Composite) of scart terminal / (S) switch
93	PL0/SDA1	SDAI	12C Serial	12C control lines
94	PL1/SDA0	NC	–	NC
95	PL2/SCL1	SCLI	12C Serial	12C control lines
96	PL3/SCL0	NC	–	NC
97	PL4	CTS	I	RS-232C clear to send input
98	PL5	DTR	O	RS-232C clear to send output
99	PL6/UC0	NC	O	NC
100	VSS	GND	–	Ground

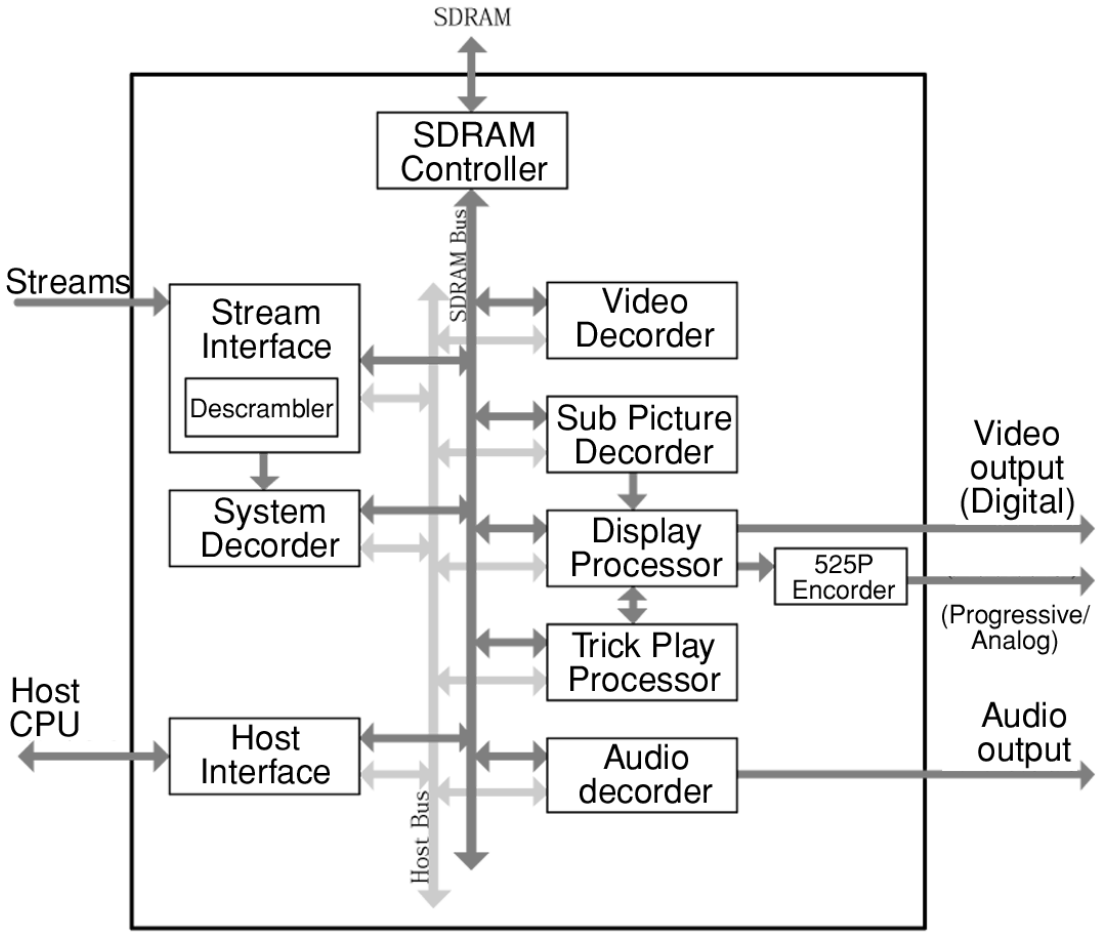
No.	Mark	Pin Name	I/O	Pin Function
101	PK0/TIN0	XVQERST	O	VQE3 reset signal
102	PK1/TIN1	XCSPRO1	–	Serial communication enable of the progressive converter IC
103	PK2/TIN2	XCSVQE5	–	Serial communication enable of VQE5 IC
104	PK3/TIN3	EN16M	O	N.C.
105	PK4/TOT0	44X48	O	DAC and DASP supply clock fs 44/48 selection
106	PK5/TOT1	1394XRDY	I	N.C.
107	PK6/TOT2	AOSEL1	O	AV-1/audio DSP switch (front L/R data)
108	PK7/TOT3	P/XI	O	Progressive/Inter race change signal
109	VCC3	V+3.3D	–	Power supply
110	VCC2	V+2.5D	–	Power supply
111	PJ0/INT0	XINT0	I	
112	PJ1/INT1	XINT1	I	
113	PJ2/INT2	XIRQ10	I	MY chip interrupt #0
114	PJ3/INT3	XIRQ11	I	MY chip interrupt #1
115	PJ4/INT4	XABUSY	I	Busy signal of DSP process operation "L"
116	PJ5/INT5	THLD	I	Playback speed monitoring signal
117	PJ6/INT6	SBSY	I	Sync. signal of subcode block (period SO+SI "H")
118	PJ7/INT7	N.C.	I	N.C.
119	PI0/SI0	SSI	I	Serial bus data input
120	PI1/SO0	SSO_3V	O	Serial bus data output
121	PI2/SCK0	SSCK_3V	I	Serial bus clock input
122	PI3/SI1	RXD_3V	I	RS-232C RXD
123	PI4/SO1	TXD_3V	O	RS-232C TXD
124	PI5/SCK1	NC	O	NC
125	PH0/SI2	1394LT	O	NC
126	PH1/SO2	DSPICM	I	Audio system DSP serial communication Readv signal
127	PH2/SCK2	NC	I	NC
128	MD0	GND	–	Ground
129	MD1	GND	–	
130	MD2	GND	–	
131	VSS	GND	–	Ground
132	VCC2	V+2.5D	–	Power supply
133	VSS	GND	–	Ground
134	X1	EXTAL	O	
135	X0	XTAL	I	
136	VCC3	V+3.3D	–	Power supply
137	PC0/DREQ2	RESET1	O	Audio system DSP reset
138	PC1/DACK2	XCSADSP0	O	Chip select port for audio system DSP
139	PC2/DEOP2	XCSDF2	O	DAC chip select (for surround system L/R)
140	PB0/DREQ0	XDREQ0	I	DMA response output to BY Chip
141	PB1/DACK0	DACK0	O	DMA request input from BY Chip
142	PB2/DEOP0	ENCD	O	N.C.
143	PB3/DREQ1	XDREQ1	I	DMA response output to AV-1 Chip
144	PB4/DACK1	XDACK1	O	DMA request input from AV-1 Chip
145	PB5/DEOP1	EN_FLOW	O	N.C.
146	PB6/IOWRX	XCOMP	O	RGB/color difference change of video driver
147	PB7/IORDX	XCSDF3	O	N.C.
148	VSS	GND	–	Ground
149	PA0/CSOX	XCS20	O	Chip select output to Flash ROM
150	PA1/CS1X	XCS6	O	AV-1 Chip select

No.	Mark	Pin Name	I/O	Pin Function
151	PA2/CS2X	XCS3	O	Chip select of PD4995A (MY Chip)
152	PA3/CS3X	XCS4	O	Chip select of servo DSP
153	PA4/CS4X	XCS23	O	Chip select output to SRAM (1M)
154	PA5/CS5X	N.C.	O	N.C.
155	PA6/CS6X	N.C.	O	N.C.
156	PA7/CS7X	N.C.	O	N.C.
157	VCC3	V+3.3D	–	Power supply
158	VCC2	V+2.5D	–	Power supply
159	NMIX	–	–	V+3.3D fixed
160	HSTX	–	–	V+2.5D fixed
161	INITX	XINIT	I	
162	P80/RDY	RDY	I	
163	P81/BGRNTX	XAMUTE	I	Final stage mute of 2 ch audio output
164	P82/BRQ	XMMUTE	O	Audio multi channel mute
165	P83/RDX	XRD	O	
166	P84/WR0X	XWR0	O	
167	P85/WR1X	XWR1	O	
168	VSS	GND	–	Ground
169	P90/SYSCLK	SYSCLK	O	N.C.
170	P91	DFRST	–	DAC reset (for front L/R)
171	P92/MCLK	DFRST1	–	DAC reset (for center, surround and LFE)
172	P93	XCSDF0	O	DAC chip select (←XLAT3)
173	P94/LBAX	XCSDF1	O	DAC chip select for center, surround and LFE
174	P95/BAAX	XAQRST	O	AQE reset
175	P96	XCSAQE	O	AQE chip select
176	P97/WEX	TM ENT	I	Test mode entry

■ M65776AFP (DVDM ASSY : IC751)

- **MPEG2 Decorder IC**

● **Block Diagram**



● Pin Function

No.	Pin name	Dir.	Pin Functions
201-208	BD [7:0]	IN	Bit stream data entry pin
2	BCLK	IN	Strobe signal of BD pin (clock)
3	BDEN	IN	This order effective / invalidity of data done a sample of by BD pin. It is done a sample with a start edge of BCLK.
4	BDREQ	OUT	Data demand signal
5	BSECH	IN	This order it whether data of BD pin are with top byte of a sector.
84-87 90-95 97-102	MD [15:0]	I/O	Data transfer line with SDRAM
53-55 58-63 65, 67, 69	MA [11:0]	OUT	Address line of SDRAM
66, 68	MBA [1:0]	OUT	SDRAM bank choice line
70	DCS	OUT	Chip select of SDRAM
73	DCS2		
74	DCS3		
75	DCS4		
76	DCS5		
77	RAS	OUT	RAS (Row Address Strobe) control line of SDRAM
78	CAS	OUT	CAS (Column Address Strobe) control line of SDRAM
82	DQMU	OUT	DQM control line of SDRAM
83	DQML	OUT	DQM control line of SDRAM
80	DWE	OUT	WE control line of SDRAM
79	MCLK	OUT	Movement clock of SDRAM
183	PXCLK	OUT	27MHz pixel clock
182	PXCLKP	OUT	54MHz pixel clock
157, 158, 184-186 188-192	PD [7:0]	OUT	Digital pixel data. Y/Cb/Cr is done multiple of by 8 bit bus, and it is output.
178	CSYNC	IN	Composite SYNC signal input terminal
179	OSDKEY	OUT	OSD key flag output
177	PWD	OUT	The phase comparator output for external synchronization movement
181	HSYNC	OUT	Horizontal synchronizing signal output pin
180	VSYNC	OUT	Vertical synchronizing signal output pin
164	AO0	OUT	Serial PCM data for DAC It output Lf/Rf data.
166	AO1	OUT	Serial PCM data for DAC It output C/Sw data.
167	AO2	OUT	Serial PCM data for DAC It output Ls/Rs data.
168	AOD	OUT	Serial PCM data for DAC It is for the down mixture output.
169	AAD	OUT	Anciallary data output
176	DOCLK	OUT	PCM bit clock
159	LRCLK	OUT	Clock for channel distinction of pulse code modulation audio system data (L/R)
173	DACCLK	OUT	Exaggerated sample movement clock of DAC
161	CDBCK	IN	The pulse code modulation bit clock which is input by CDDSP
160	CDLRCK	IN	The L/R clock which is input by CDDSP

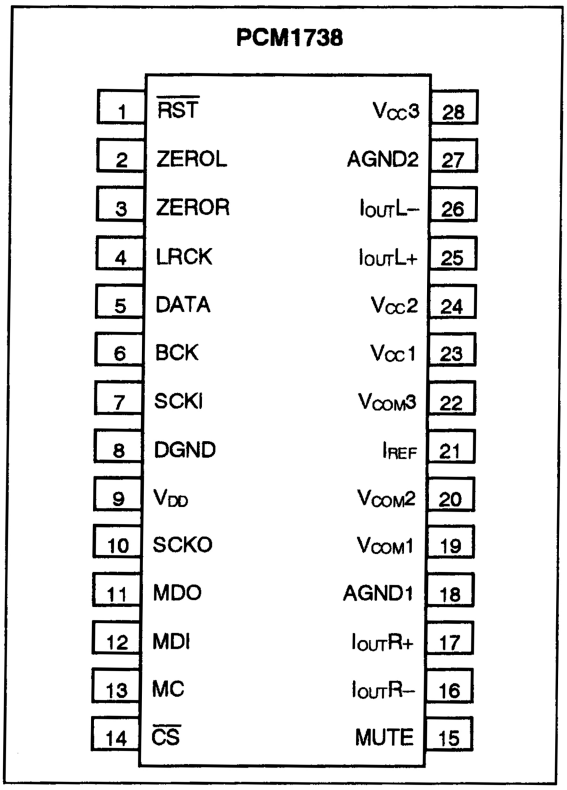
No.	Pin name	Dir.	Pin Functions
163	CDDIN	IN	PCM audio system data which are input by CDDSP
162	CDDATA	IN	Digital audio interface input
170	DOUT0	OUT	Digital audio interface output
171	DOUT1	OUT	Digital audio interface output
6-11 14-19 21-24	HD [15:0]	I/O	Data I/O pin
25, 26 29-34 36-39	HA [11:0]	IN	Address input pin
45	BHE	IN	Byte High Enable signal input pin
41	RE	IN	Read Enable signal input pin
44	WE	IN	Write Enable signal input pin
40	CS	IN	Chip Select signal input pin
46	RDY	OUT	The acknowledge signal which shows that readout of data or a note was completed
47	INT1	OUT	It is an interrupt request signal for outside CPU from M65776AFP
48	INT2		
49	INT3		
51	DREQ	OUT	DMA request signal for OSD BitMap transfer
52	DACK	IN	DMA acknowledge signal for OSD BitMap transfer
194, 195	HMODE [1:0]	IN	Host interface mode of operation setting pin
117	IREF	IN	Reference electric current input pin
115	AVRI	IN	Reference voltage input pin
120	BIAS1	IN	Bias voltage impression pin of current source
118	BIAS2		
119	PAY	OUT	Analog electric current output pin (for Y)
116	PAB	OUT	Analog electric current output pin (for Pb)
122	PAR	OUT	Analog electric current output pin (for Pr)
114	DAOUTB	OUT	Be connected to an analog ground.
113, 121, 123	AVDD33	–	3.3V analog power supply
124	AGND33	–	Analog ground
106	CLKIN	IN	System clock input terminal It input 27MHz clock.
105	CLKO	OUT	27MHz clock output
172	ACLKI	IN	Audio system clock input terminal
193	RESET	IN	Hardware reset terminal
196, 197, 200	TEST [2:0]	IN	Fix it in "L" potential.
12, 27, 42, 56, 71, 88, 103, 134, 155, 174, 198	VDD18	–	1.8V power supply terminal
13, 28, 43, 57, 72, 89, 104, 135, 156, 175, 199	VDD33	–	3.3V power supply terminal

No.	Pin name	Dir.	Pin Functions
1, 20, 35, 50, 64, 81, 96, 112, 125, 145, 165, 187	GND	–	Ground terminal
107	AVDD18	–	1.8V power supply terminal for inside PLL
108	AGND18	–	Ground terminal for inside PLL
109-111 126-133 136-144 146-154	NC0	NC	

■ PCM1738EG-3 (JACB ASSY : IC301)

• D/A Converter IC

● Pin Arrangement



● Pin Function

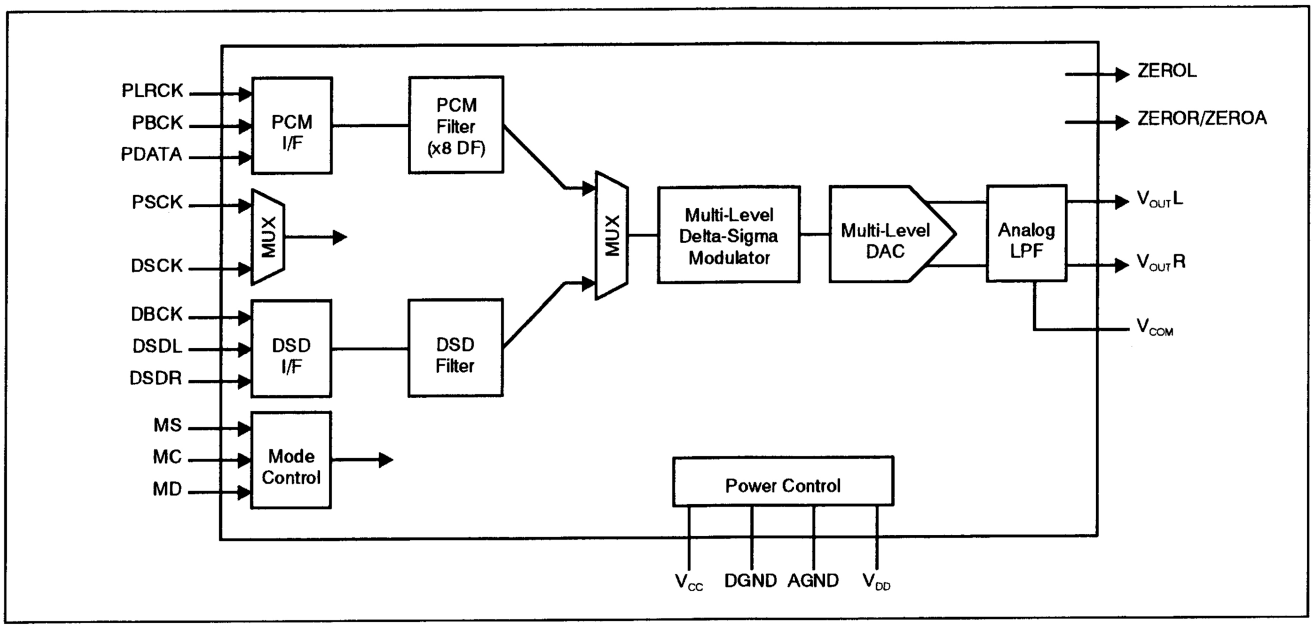
PIN	NAME	TYPE	DESCRIPTIONS
1	$\overline{RST}$	IN	Reset (1)
2	ZEROL	OUT	Zero Flag for L-channel
3	ZEROR	OUT	Zero Flag for R-channel
4	LRCK	IN	Left and Right Clock (f_S) Input for Normal operation. WDCK clock input in External DF mode. Connected to GND in DSD mode. (1)
5	DATA	IN	Serial Audio Data Input for Normal operation. L-channel audio data input for External DF and DSD modes. (1)
6	BCK	IN	Bit Clock. Input. Connected GND for DSD mode. (1)
7	SCKI	IN	System Clock Input. BCK (64 f_S) clock input for DSD mode (1)
8	DGND	-	Digital Ground
9	V_{DD}	-	Digital Supply, +3.3 V
10	SCKO	OUT	System Clock Output
11	MDO	OUT	Serial data output for function control register (2)
12	MDI	IN	Serial data input for function control register (1)
13	MC	IN	Shift Clock for function control register (1)
14	$\overline{CS}$	IN	Mode control chip select and latch signal. (1)
15	MUTE	IN	Analog output mute control for normal operation R-channel audio data input for external DF mode and DSD mode. (1)
16	$I_{OUT}R-$	OUT	R-channel Analog Current Output –
17	$I_{OUT}R+$	OUT	R-channel Analog Current Output +
18	AGND1	-	Analog Ground.
19	$V_{COM}1$	-	Internal bias de-coupling pin
20	$V_{COM}2$	-	Common voltage for I/V
21	I_{REF}	-	Output current reference bias pin. Connect 16KΩ resistor to GND
22	$V_{COM}3$	-	Internal bias de-coupling pin
23	$V_{CC}1$	-	Analog Supply, +5.0 V
24	$V_{CC}2$	-	Analog Supply, +5.0 V
25	$I_{OUT}L+$	OUT	L-channel Analog Current Output +
26	$I_{OUT}L-$	OUT	L-channel Analog Current Output –
27	AGND2	-	Analog Ground
28	Vcc3	-	Analog Power Supply, +5.0V

NOTES:
(1) Schmitt trigger input, 5 V tolerant.
(2) Tristate output.

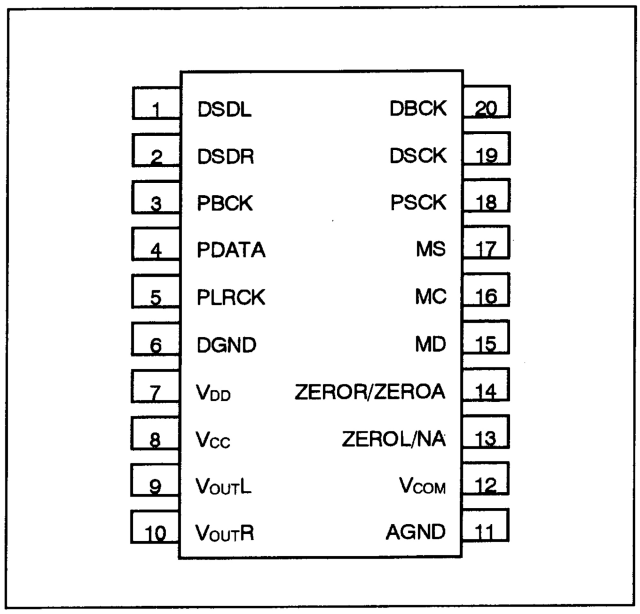
■ DSD1702EG (JACB ASSY : IC401, IC501)

• D/A Converter IC

● Block Diagram



● Pin Arrangement



● Pin Function

PIN	NAME	TYPE	DESCRIPTIONS
1	DSDL	IN	Audio data digital input (DSD L-channel) (1)
2	DSDR	IN	Audio data digital input (DSD R-channel) (1)
3	PBCK	IN	Audio data bit clock input. (PCM) (1)
4	PDATA	IN	Audio data digital input. (PCM) (1)
5	PLRCK	IN	Audio data latch enable input. (PCM) (1)
6	DGND	-	Digital ground.
7	V_{DD}	-	Digital power supply, + 3.3 V.
8	V_{CC}	-	Analog power supply, + 5 V.
9	$V_{OUT}L$	OUT	Analog output for L-channel.
10	$V_{OUT}R$	OUT	Analog output for R-channel.
11	AGND	-	Analog ground.
12	V_{COM}	-	Common voltage decoupling.
13	ZEROR/ZEROA	OUT	Zero flag output for R-channel / Zero flag output for L/R-channel.
14	ZEROL/NA	OUT	Zero flag output for L-channel / No assign.
15	MD	IN	Mode control data Input. (2)
16	MC	IN	Mode control clock input. (2)
17	MS	IN	Chip Select for Mode control. (2)
18	PSCK	IN	System clock input. (PCM) (1)
19	DSCK	IN	System clock input. (DSD) (1)
20	DBCK	IN	Audio data bit clock input. (DSD) (1)

Note:

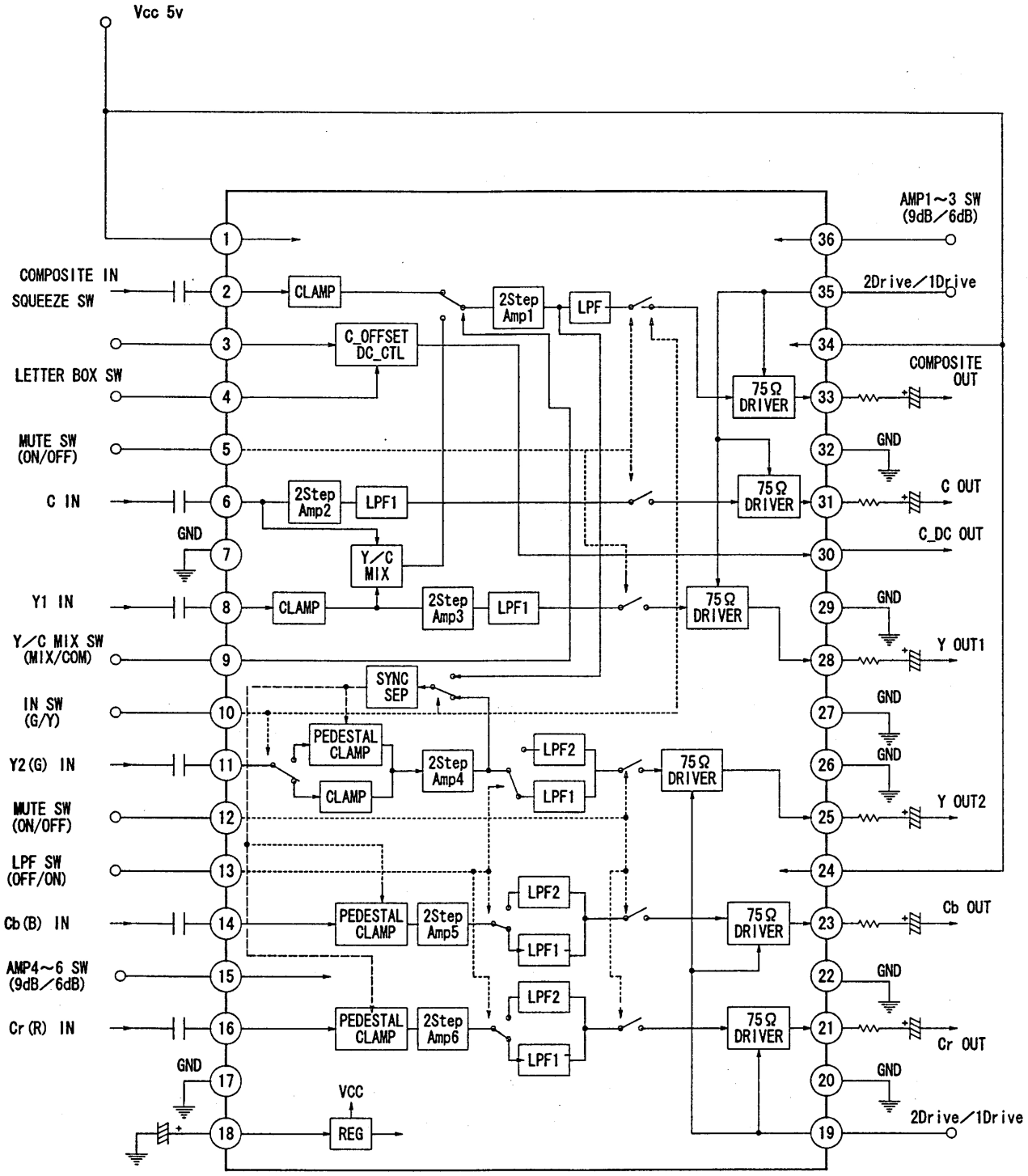
(1) Schmidt trigger input, 5 V tolerant.

(2) Schmidt trigger input with internal pull-down, 5 V tolerant.

■ LA73054 (JACB ASSY : IC701)

- **DVD Video Amplifier**

● Block Diagram



● Pin Function

No.	Pin Functions		0– 0.7V (LOW)	2.6– 5V (HIGH)
36	AMP-GAIN change for composite/S		6 dB	9 dB
15	AMP-GAIN change for component		6 dB	9 dB
35	Drive electric current change for composite/S		2 system drive	1 system drive
19	Drive electric current change for component		2 system drive	1 system drive
5	Mute control for composite/S	In 10 pin LOW	It is not do mute	33, 31, 28 pin mute
		In 10 pin HIGH	It is not do mute	31, 28 pin mute
12	Mute control for component		It is not do mute	25, 23, 21 pin mute
9	The control of Y/C– MIX		In composite	In Y/C– MIX
10	11 pin input form change		In the component input	In the baseband input
13	LPF characteristic change for component		Inter race correspondence	Progressive correspondence

2 pin falls to GND in Y/C-MIX.

11 pin is clamp, and the Y signal input, 14, 16 pin input a CB, CR signal into NTSC (in the component input) with pedestal clamp.

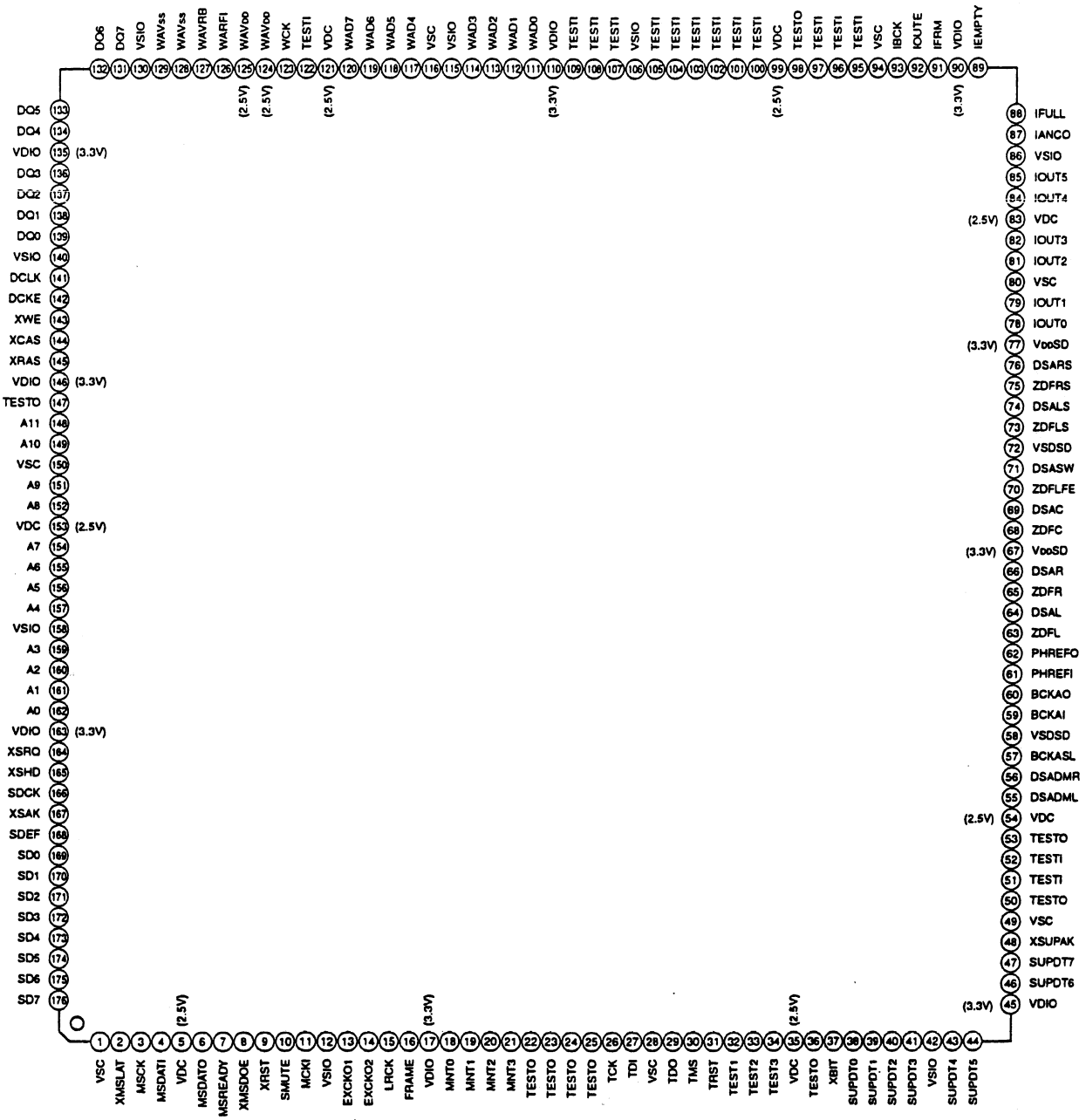
8 pin is clamp, and the Y signal input, 11, 14, 16 pin input a R, G, B signal into PAL (in the baseband input) with pedestal clamp.

It prohibit mute of 5 pin when It do Y/C-MIX in PAL (in the baseband input).

■ CXD2753R (SACDB ASSY : IC901)

• SACD Decorder

● Pin Arrangement



● Pin Function

No.	Pin Name	I/O	Pin Function
1	VSC	-	Ground terminal for core
2	XMSLAT	I	Latched input terminal for microcomputer serial communication
3	MSCK		Shift clock input terminal for microcomputer serial communication
4	MSDAI		Data entry terminal for microcomputer serial communication
5	VDC	-	Power supply terminal for core
6	MSDATO	O	Data output terminal for microcomputer serial communication
7	MSREADY		Output preparation completion flag for microcomputer serial communication
8	XMSDOE		Output enable terminal for microcomputer serial communication
9	XRST	I	Reset terminal resets the whole IC with "L".
10	SMUTE	Ipd	Software mute removes audio out with "L" with "H" a soft mute terminal.
11	MCKI	I	Master clock input terminal
12	VSIO	-	Ground terminal for I/O
13	EXCKO1	O	Outside output clock terminal 1
14	EXCKO2		Outside output clock terminal 2
15	LRCK		1Fs (44.1kHz) clock output terminal
16	FRAME		Frame signal output terminal
17	VDIO	-	Power supply terminal for I/O
18	MNT0	O	Monitor output terminal
19	MNT1		
20	MNT2		
21	MNT3		
22	TESTO		Output terminal for test
23			
24			
25			
26	TCK	I	It is fixation in "L" a clock input terminal for test.
27	TDI	Ipu	Input terminal for test
28	VSC	-	Ground terminal for core
29	TDO	O	Output terminal for test
30	TMS	Ipu	Input terminal for test
31	TRST		Reset terminal for test
32	TEST1	I	It is fixation in "L" a clock input terminal for test.
33	TEST2		
34	TEST3		
35	VDC	-	Power supply terminal for core
36	TESTO	O	Output terminal for test
37	XBIT		DST connection monitor terminal
38	SUPDT0		Supplementary data output terminal (LSB)
39	SUPDT1		Supplementary data output terminal
40	SUPDT2		
41	SUPDT3		
42	VSIO	-	Ground terminal for I/O
43	SUPDT4	O	Supplementary data output terminal
44	SUPDT5		
45	VDIO	-	Power supply terminal for I/O
46	SUPDT6	O	Supplementary data output terminal
47	SUPDT7		Supplementary data output terminal (MSB)
48	XSUPAK		Supplementary data output terminal
49	VSC	-	Ground terminal for core
50	TESTO	O	Output terminal for test

No.	Pin Name	I/O	Pin Function
51	TESTI	I	It is fixation in "L" a test input terminal.
52			
53	TESTO	O	Output terminal for test
54	VDC	-	Power supply terminal for core
55	DSADML	O	DSD data output terminal for Lch Down Mix
56	DSADMR		DSD data output terminal for Rch Down Mix
57	BCKASL	I	Input and output choice terminal of a 1 bit clock for DSD data output.L= input (slave), H = output (master).
58	VSDSD	-	Ground terminal for DSD data output
59	BCKAI	I	Bit clock input terminal for DSD data output
60	BCKAO	O	Bit clock output terminal for DSD data output
61	PHREFI	I	Phase reference signal input terminal for DSD output phase modulation
62	PHREFO	O	Phase reference signal output terminal for DSD output phase modulation
63	ZDFL		Zero Lch data search flag
64	DSAL		DSD data output terminal for Lch loud speaker
65	ZDFR		Zero Rch data search flag
66	DSAR		DSD data output terminal for Rch loud speaker
67	VDDSD	-	Power supply Mizuko for DSD data output
68	ZDFC	O	Zero Cch data search flag
69	DSAC		DSD data output terminal for Cch loud speaker
70	ZDFLFE		Zero LFEch data search flag
71	DSASW		DSD data output terminal for SWch loud speaker
72	VSDSD	-	Ground terminal for DSD data output
73	ZDFLS	O	Zero LSch data search flag
74	DSALS		DSD data output terminal child for LSch loud speaker
75	ZDFRS		Zero RSch data search flag
76	DSARS		DSD data output terminal for RSch loud speaker
77	VDDSD	-	Power supply Mizuko for DSD data output
78	IOUT0	O	Data output terminal 0 for IEEE1394 link tip I/F
79	IOUT1		Data output terminal 1 for IEEE1394 link tip I/F
80	VSC	-	Ground terminal for core
81	IOUT2	O	Data output terminal 2 for IEEE1394 link tip I/F
82	IOUT3		Data output terminal 3 for IEEE1394 link tip I/F
83	VDC	-	Power supply terminal for co
84	IOUT4	O	Data output terminal 4 for IEEE1394 link tip I/F
85	IOUT5		Data output terminal 5 for IEEE1394 link tip I/F
86	VSIO	-	Ground terminal for I/O
87	IANCO	O	Transmission information data output terminal for IEEE1394 link tip I/F
88	IFULL	I	Data transmission hold demand signal input terminal for IEEE1394 link tip I/F
89	IEMPTY		High speed transmission demand signal input terminal for IEEE1394 link tip I/F
90	VDIO	-	Power supply terminal for I/O
91	IFRM	O	Frame reference signal output Mizuko for IEEE1394 link tip I/F
92	IOUTE		Enable signal output terminal for IEEE1394 link tip I/F
93	IBCK		Data transmission clock output terminal for IEEE1394 link tip I/F
94	VSC	-	Ground terminal for core
95	TESTI	I	It is fixation in "H" a test input terminal.
96			It is fixation in "L" a test input terminal.
97		Ipu	It is fixation in "H" a test input terminal.
98	TESTO	O	Output terminal for test
99	VDC	-	Power supply terminal for co
100	TESTI	I	It is fixation in "L" a test input terminal.

No.	Pin Name	I/O	Pin Function
101	TESTI	I	It is fixation in "L" a test input terminal.
102			
103			
104			
105			
106	VSIO	-	Ground terminal for I/O
107	TESTI	I	It is fixation in "L" a test input terminal.
108			
109			
110	VDIO	-	Power supply terminal for I/O
111	WAD0	I	Outside A/D data entry terminal for PSP Physical Disc Mark search (LSB)
112	WAD1		Outside A/D data entry terminal for PSP Physical Disc Mark search
113	WAD2		
114	WAD3		
115	VSIO	-	Ground terminal for I/O
116	VSC	-	Ground terminal for core
117	WAD4	I	Outside A/D data entry terminal for PSP Physical Disc Mark search
118	WAD5		
119	WAD6		
120	WAD7		Outside A/D data entry terminal for PSP Physical Disc Mark search (MSB)
121	VDC	-	Power supply terminal for core
122	TESTI	I	It is fixation in "L" a test input terminal.
123	WCK		Movement clock for PSP Physical Disc Mark search
124	WAVDD	-	A/D power supply terminal for PSP Physical Disc Mark search
125			
126	WARFI	Ai	Analog RF signal input terminal for PSP Physical Disc Mark search
127	WAVRB		A/D bottom reference terminal for PSP Physical Disc Mark search
128	WAVSS	-	A/D ground terminal for PSP Physical Disc Mark search
129			
130	VSIO	-	Ground terminal for I/O
131	DQ7	I/O	SDRAM data input-output terminal (MSB)
132	DQ6		SDRAM data input-output terminal
133	DQ5		
134	DQ4		
135	VDIO	-	Power supply terminal for I/O
136	DQ3	I/O	SDRAM data input-output terminal
137	DQ2		
138	DQ1		
139	DQ0		SDRAM data input-output terminal (LSB)
140	VSIO	-	Ground terminal for I/O
141	DCLK	O	Clock output terminal for SDRAM
142	DCKE		Clock enable output terminal for SDRAM
143	XWE		Wright enable output terminal for SDRAM
144	XCAS		Column address strobe output terminal for SDRAM
145	XRAS		Row address strobe output terminal for SDRAM
146	VDIO	-	Power supply terminal for I/O
147	TESTO	O	Output terminal for test
148	A11		Address output terminal for SDRAM (MSB)
149	A10		Address output terminal for SDRAM
150	VSC	-	Ground terminal for core

No.	Pin Name	I/O	Pin Function
151	A9	O	Address output terminal for SDRAM
152	A8		
153	VDC	-	Power supply terminal for core
154	A7	O	Address output terminal for SDRAM
155	A6		
156	A5		
157	A4		
158	VSIO	-	Ground terminal for I/O
159	A3	O	Address output terminal for SDRAM
160	A2		
161	A1		
162	A0		Address output terminal for SDRAM (LSB)
163	VDIO	-	Power supply terminal for I/O
164	XSRQ	O	Data request output terminal to input into a front end processor
165	XSHD	I	Input terminal of a header flag output by a front end processor
166	SDCK		Input terminal of a data carrier clock output by a front end processor
167	XSAK		Input terminal of data partial response flag output by a front end processor
168	SDEF		Input terminal of error flag output by a front end processor
169	SD0		The stream data input terminal which is output by a front end processor (LSB)
170	SD1		The stream data input terminal which is output by a front end processor
171	SD2		
172	SD3		
173	SD4		
174	SD5		
175	SD6		
176	SD7		The stream data input terminal which is output by a front end processor (MSB)

Ipu : Pull-up input, Ipd : Pull-down input, Ai : Analog input

■ PE5314B (FLKY ASSY : IC101)

• FL Controller

● Pin Function

No.	Signal name	Dir.	Pin Functions
1	V_{DD1}	–	Positive Power Supply (3.3 V)
2	V_{SS1}	–	Ground Potential
3	X1	IN	Crystal Connection for Main System Clock Oscillation
4	X2	–	
5	IC	–	Internally Connected (Directly connect to VSS1)
6	RESET	IN	Reset Input
7	SCK1	IN	Serial Clock Input of Serial Interface
8	SI1	IN	Serial Data Input of Serial Interface
9	SO1	OUT	Serial Data Output of Serial Interface
10	XRDY	OUT	Hand-shake (Ready) Output of Serial Interface
11	POWER ON	OUT	Power Control Output
12	RESET OUT	OUT	System Reset Output
13	RESERVE OUT	OUT	Reserved (NC on this model)
14	LED8	OUT	LED Port 8 (NC on this model)
15	HALT	IN	Halt Port "NC" : Use Halt Mode
16	ACK	IN	Hand-shake (Acknowledge) Input of Serial Interface (Interrupt)
17	SEL IR	IN	Remote Control Input (Timer input of 8-bit remote control timer)
18	A_{VSS}	–	Ground Potential for A/D Converter
19	MS1	IN	Destination (of player) Select (Analog Input for A/D Converter)
20	NC	–	NC
21	KEY1	IN	Key Input 1 (Analog input for A/D converter)
22	KEY0	IN	Key Input 0 (Analog input for A/D converter)
23	VSS0	–	Ground Potential to Ports
24	AVDD	–	Analog Power/Reference Voltage Input to A/D Converter (3.3 V)
25	VDD0	–	Positive Power Supply to Ports (3.3 V)
26	MS0_2	IN	Model (of player) Select (Set with a combinaition of this 3 ports)
27	MS0_1		
28	MS0_0		
29	LED7	OUT	LED Port 7
30	LED(STAND BY)	OUT	Stand By LED Port
31	PWSW	IN	Primary Switch State Input "H" : ON "L" : OFF
32	TES	IN	"H" : No System Reset mode "L" : General mode
33	OEM	IN	"H" : OEM Model "L" : Pioneer Model
34	MIC IN	IN	Detection of Microphone "H" : Microphone connected
35	CHECKER	IN	"H" : Checker Mode "L" : General mode
36	ON POWER	IN	"H" : Primary Power Switch Model "L" : Secondary Power Switch Model
37	FL SET2	IN	FL-Controller Mode Select FL SET1 / 2 = "H" / "H" : Other model FL SET1 / 2 = "H" / "L" : Other model FL SET1 / 2 = "L" / "H" : Other model FL SET1 / 2 = "L" / "L" : DV-555, 656A, 757Ai (This model)
38	FL SET1		
39	TEST2	OUT	Test Port
40	LED6	OUT	LED Port 6

No.	Signal name	Dir.	Pin Function
41	LED5	OUT	LED Port 5
42	LED4		LED Port 4
43	LED3		LED Port 3 (NC on this model)
44	LED2		LED Port 2 (NC on this model)
45	LED1		LED Port 1 (NC on this model)
46	LED0		LED Port 0 (NC on this model)
47	TEST1	OUT	Test Port
48	NC	–	NC
49	1394RST	OUT	1394 Host Controller Reset Output
50	NC	–	NC
51	P16	OUT	FIP Segment 16 Output
52	P15	OUT	FIP Segment 15 Output
53	NC	–	NC
54	P14	OUT	FIP Segment 14 Output
55	P13		FIP Segment 13 Output
56	P12		FIP Segment 12 Output
57	P11		FIP Segment 11 Output
58	P10		FIP Segment 10 Output
59	VDD2	–	Positive Power Supply to FIP Controller/Driver (3.3 V)
60	VLOAD	–	Pull-down Resistor Connection of FIP Controller/Driver (-28V)
61	P9	OUT	FIP Segment 9 Output
62	P8		FIP Segment 8 Output
63	P7		FIP Segment 7 Output
64	P6		FIP Segment 6 Output
65	P5		FIP Segment 5 Output
66	P4		FIP Segment 4 Output
67	P3		FIP Segment 3 Output
68	P2		FIP Segment 2 Output
69	P1		FIP Segment 1 Output
70	G11	OUT	FIP Grid 11 Output
71	G10		FIP Grid 10 Output
72	G9		FIP Grid 9 Output
73	G8		FIP Grid 8 Output
74	G7		FIP Grid 7 Output
75	G6		FIP Grid 6 Output
76	G5		FIP Grid 5 Output
77	G4		FIP Grid 4 Output
78	G3		FIP Grid 3 Output
79	G2		FIP Grid 2 Output
80	G1		FIP Grid 1 Output

■ PE5286A (DVDM ASSY : IC701)

• DVD Data Processor

● Pin Function

No.	Pin name	Dir.	Pin Functions
3, 40, 50, 54, 84, 103, 107, 145, 154, 158, 207	VDD3.3	–	It is a power supply of digital circuit. Be connected to +3.3V.
15, 18, 27, 53, 64, 74, 78, 92, 104, 130, 157, 164, 183, 191, 208	VDD2.5	–	It is a power supply of digital circuit. Be connected to +2.5V.
1, 2, 16, 17, 26, 41, 51, 52, 63, 73, 79, 85, 91, 105, 106, 131, 144, 150, 155, 156, 178, 182, 190	GND	–	It is a ground of digital circuit.
167, 171, 175	NC	–	It is a non-use pin. Fix it in GND or VDD.
165 166	AVDD	–	It is a power supply supply terminal for built-in analog-to-digital converter. Supply +2.5V (analog).
176 177	AGND	–	It is a GND terminal for built-in D/A converter.
6	BUNRI	IN	It is a separation test control terminal of inside RAM. Input LOW in use usually.
90	TMC1	IN	It is a test terminal. Input LOW in use usually.
148	TMC2	IN	
4	DMCK/RF_A	IN	It is the system clock input of DVD/CD-ROM decoder. Input 10-54MHz.
189	CKCD	IN	It is master clock of an audio system I/F block. In audio out of a CD, input 16.9MHz of reference clock.
5	DMACKI/PD4	IN	Fix unused time (unused usually) in GND or VDD.
149	VCOCLK	IN	With system clock of spindle demodulator, it is connected to VCO of outside charge account.
161	XRESET	IN	By the input of a LOW level, It initialize the whole large scale integrated circuit system.
135	SA19	I/O	Connect address bus of central processing unit.
134	SA18		
133	SA17		
132	SA16		
129	SA15		
128	SA14		
127	SA13		
126	SA12		
125	SA11		
124	SA10		
123	SA9		

No.	Pin name	Dir.	Pin Functions
122	SA8	IN	Connect address bus of central processing unit.
121	SA7		
120	SA6		
119	SA5		
118	SA4		
117	SA3		
116	SA2		
115	SA1		
114	SA0		
99	SAD7	I/O	Connect a data bus of central processing unit.
100	SAD6		
101	SAD5		
102	SAD4		
108	SAD3		
109	SAD2		
110	SAD1		
111	SAD0		
97	XSRD	IN	Be connected to a RD signal of central processing unit.
98	XSWR	IN	Be connected to a WR signal of central processing unit.
96	XSCL1	IN	It is chip select signal from central processing unit. XSRD/XSWR becomes effective at the time of LOW this signal.
95	XSWAIT	OUT	It is the WAIT output for central processing unit. This terminal must leave access from central processing unit at the time of LOW.
94	XSDREQ	OUT	It is a DMA demand for central processing unit. LOW level hip of this terminal falls down and activates DMA transfer with an edge.
93	SDACK	IN	It is DMA answer back. Data are output with HIGH this signal by SAD (7:0).
112	XIRQ10	OUT	It demand interrupt for central processing unit with LOW. Both terminals can set it with a register whether they output it.
113	XIRQ11		
141	FGPL/PE3	IN	Input a turn pulse from spindle motor.
147	FPWM	OUT	It is 7bitPWM output terminal for FG servo. It is the 3 value output of HIGH,LOW, high impedance.
146	VPWM	OUT	It is 5bitPWM output terminal for speed servo. It is the 3 value output of HIGH,LOW, high impedance.
143	PPWM	OUT	It is pulse width modulation output terminal for phase servo. It is the 3 value output of HIGH,LOW, high impedance.
142	RERR	OUT	It is control output for rough servo. It is the 3 value output of HIGH,LOW, high impedance.
31	PA7	I/O	It is general-purpose I/O port. By setting of a $70 register, You can select a function. CDDO inputs a digital out signal from a CD decoder. DIFOUT is digital audio output terminal based on IEC958. BCA is terminal to input a BCA code into. RWDIN is terminal to input a WOBBLE signal into. BCA/RWDIN terminal becomes necessary with RW revitalization machines.
32	PA6		
33	PA5		
34	PA4		
35	CDDO/PA3		
36	DIFOUT		
196	BCA/PA1		
195	RWDIN/PA0		

No.	Pin name	Dir.	Pin Functions
138	PD7/STATUS2	OUT	It output a various monitor signal (STATUS (2:0)). By setting of a $ 70 register, You can use it as a general-purpose I/O port port.
139	PD6/STATUS1		
140	PD5/STATUS0		
151	DUTY50	OUT	It always output a pulse of duty 50%. It give reference voltage of a various PWD signal of the recovery system.
160	ASC	OUT	It output frequency error of a sink period as a PWD pulse.
153	APC	OUT	It output a phase error of phase locked loop as a PWD pulse.
159	ATC	OUT	It output a direct current error of a RF signal as a PWD pulse.
152	AFC	OUT	It output VC OCL k and frequency error of reference clock as a PWD pulse. It is the 3 value output of HIGH,LOW, high impedance.
163	DEFECT/PE1	IN	It is the diffect signal input from the outside. Then a phase error of phase locked loop outputs this terminal in HIGH (APC), and it is done front value hold.
162	T_DET/PC7	OUT	It output a tangential-tilt search result as a pulse width modulation pulse.
70	DA13	OUT	It is address signal of DRAM for a VBR buffer.
71	DA12		
72	DA11		
75	DA10		
76	DA9		
77	DA8		
80	DA7		
81	DA6		
82	DA5		
83	DA4		
86	DA3		
87	DA2		
88	DA1		
89	DA0		
39	DD15	I/O	It is a data bus of DRAM for a VBR buffer.
42	DD14		
43	DD13		
44	DD12		
45	DD11		
46	DD10		
47	DD9		
48	DD8		
49	DD7		
55	DD6		
56	DD5		
57	DD4		
58	DD3		
59	DD2		
60	DD1		
61	DD0		

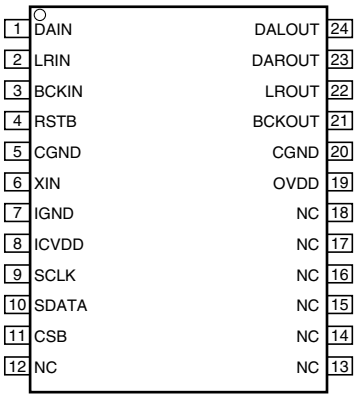
No.	Pin name	Dir.	Pin Functions
69	XDRAS	OUT	It is a RAS signal of DRAM of a VBR buffer.
67	XDCAS/XDCASL	OUT	It is a CAS signal of DRAM of a VBR buffer.
66	XDOE/DQML	OUT	It is an OE signal of DRAM of a VBR buffer.
65	XDWE	OUT	It is a WE signal of DRAM of a VBR buffer.
13	SDATA7	OUT	It is a data output bus of a VIDEO_DMA channel. Be connected to MPEG decoder.
14	SDATA6		
19	SDATA5		
20	SDATA4		
21	SDATA3		
22	SDATA2		
23	SDATA1		
24	SDATA0		
29	SREQ	IN	It is a data transfer demand terminal of a VIDEO_DMA channel. Be connected to MPEG decoder. You can change polarity by setting.
25	XSACK/PC5	OUT	It is a transfer reply terminal of a VIDEO_DMA channel. Be connected to MPEG decoder. Output form varies with setting.
28	XWR	OUT	It is a transfer reply terminal of a VIDEO_DMA channel. Be connected to MPEG decoder. Output form varies with setting.
30	XAVTRM/PC6	OUT	It is a signal to show the top of a sector of transfer data of a VIDEO_DMA channel in.
7	DSPA0/PC0	OUT	When it connects Motorola Digital Signal Processor as destination of an AUDIO_DMA channel, it is the signal which gives a DMA address to Motorola Digital Signal Processor.
8	DSPA1/PC1		
9	DSPA2/PC2		
206	ASDATA0/PB0	I/O	It is general-purpose I/O port. By setting of a $70 register, It become a data output bus of an AUDIO_DMA channel besides a port.
205	ASDATA1/PB1		
204	ASDATA2/PB2		
203	ASDATA3/PB3		
202	ASDATA4/PB4		
201	ASDATA5/PB5		
200	ASDATA6/PB6		
199	ASDATA7/PB7		
10	XAWR	OUT	It is a transfer reply terminal of an AUDIO_DMA channel. Output form varies with setting.
11	XASACK	OUT	It is a transfer reply terminal of an AUDIO_DMA channel. Output form varies with setting.
12	ASREQ	IN	It is a transfer demand terminal of an AUDIO_DMA channel. You can change polarity by setting.
192	BCK	OUT	It is the bit clock output to DAC.
193	LRCK	OUT	It is the LRCK signal output to DAC.
194	ADATA0	OUT	It is the serial data output to DAC.
187	CDBCK	IN	It input a bit clock from a CD decoder. Prospective frequency is 2.1168MHz(48fs).
186	CDLR	IN	It input a LRCK signal from a CD decoder.
185	CDDT	IN	It input audio system data from a CD decoder.
181	WFCK	IN	It is frame clock signal of a CD.
180	SCOR	IN	It is input terminal of assistant code sink of a CD.

No.	Pin name	Dir.	Pin Functions
179	SBSO	IN	It is an assistant code data input terminal of a CD.
184	EXCK	OUT	It is a shift clock making timeliness to send data forth on a SBSO terminal.
188	C2FI/PE2	IN	It is input terminal of C2 error flag from a CD decoder.
136	FSX/STATUS4	I/O	It input a FSX signal from a CD decoder. FSX signal is 7.35Khz at normal speed with frame alignment signal of error correction of CIRC. By setting of a $7F register, It become the internal monitor output (STATUS 4).
137	EFLG/STATUS3	I/O	It input an EFLG signal from a CD decoder. An EFLG signal is a monitor signal of error correction processing movement of CIRC. By setting of a $7F register, It become the internal monitor output (STATUS 3).
172	AIN	IN	It is analog RF signal input terminal to built-in A/D converter.
168	VRT	IN	It is reference voltage input terminal of built-in A/D converter.
169	VRTS	OUT	Connect with VRT.
170	VRC	OUT	It is center voltage output terminal of built-in A/D converter.
174	VRB	IN	It is reference voltage input terminal of built-in A/D converter.
173	VRBS	OUT	Connect with VRB.
37	CKE/PD3	OUT	It is an Enable signal of SDCLK.
38	CSB/PD2	OUT	It is chip select signal of SDRAM.
62	SDCLK	OUT	It is a terminal outputting a movement clock of SDRAM.
68	XCASH/DOMH	OUT	When it uses DRAM of bus 16 wide bit, it is a CAS signal of high rank 8bit.
197	VREQEN/PD1	I/O	It is an Enable signal of Video-REQ.
198	AREQEN/PD0	I/O	It is an Enable signal of Audio-REQ.

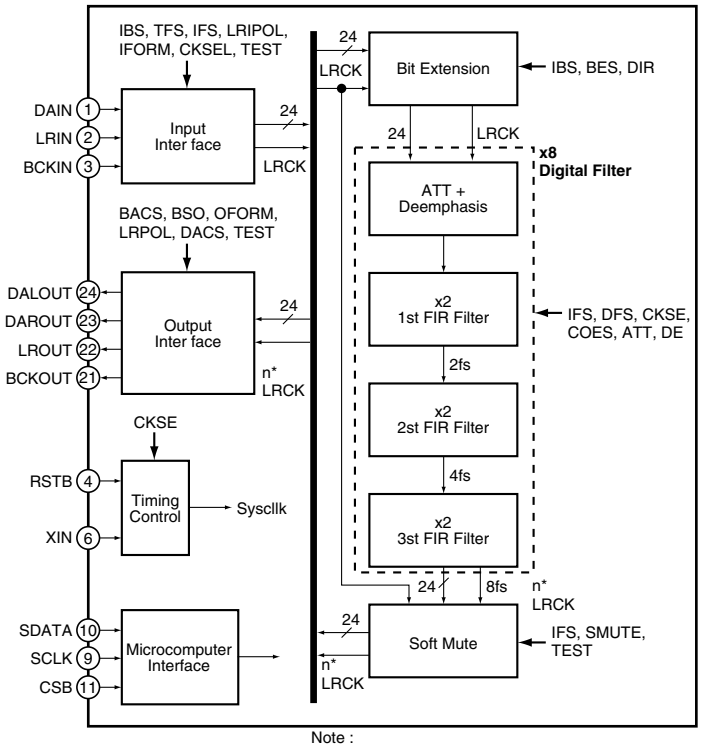
■ PD0274A (DVDM ASSY : IC552)

• Audio Quality Enhancer (AQE)

● Pin Arrangement



● Block Diagram



Note :
"n" in the Block diagram expresses the rate to sample

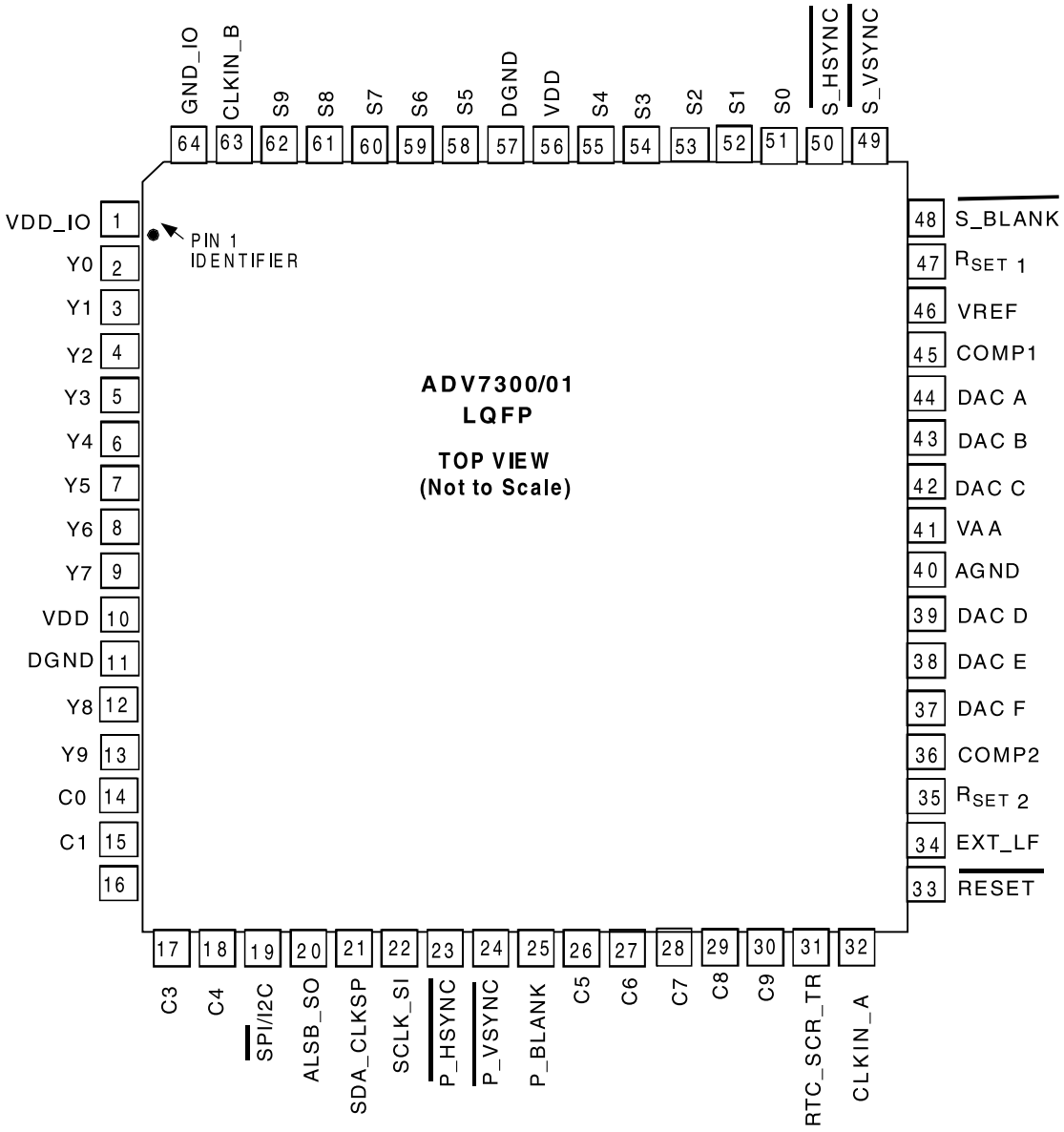
● Pin Function

No.	Name	I/O	Pin Function
1	DAIN	I	Audio data input
2	LRIN	I	L/R clock input
3	BCKIN	I	Bit clock input (48fs/64fs)
4	RSTB	I	System reset "0" = Reset
5	CGND	–	Ground (0V) for Core
6	XIN	I	System clock input (128fs/192fs/256fs/384fs/512fs/768fs)
7	IGND	–	Ground (0V) for Input Buffer
8	ICVDD	–	Power supply (3.3V) for Core and Input Buffer
9	SCLK	I	Microcomputer interface clock input
10	SDATA	I	Microcomputer interface data input
11	CSB	I	Microcomputer interface chip select input "0" = Enable, "1" = Disenable
12	NC	I	No connection
13	NC		
14	NC		
15	NC		
16	NC		
17	NC		
18	OVDD	–	Power supply (3.3V) for Output Buffer
19	OGND	–	Ground (0V) for Output Buffer
20	CGND	–	Ground (0V) for Core
21	BCKOUT	O	Bit clock output (48fs/64fs)
22	LROUT	O	L/R clock output. WCLK output at PCM1704.
23	DAROUT	O	R ch audio data output
24	DALOUT	O	L ch audio data output or L/R ch multiplex output

■ ADV7300AKST (DVDM ASSY : IC831)

• Video Encoder IC

● Pin Arrangement



● Pin Function

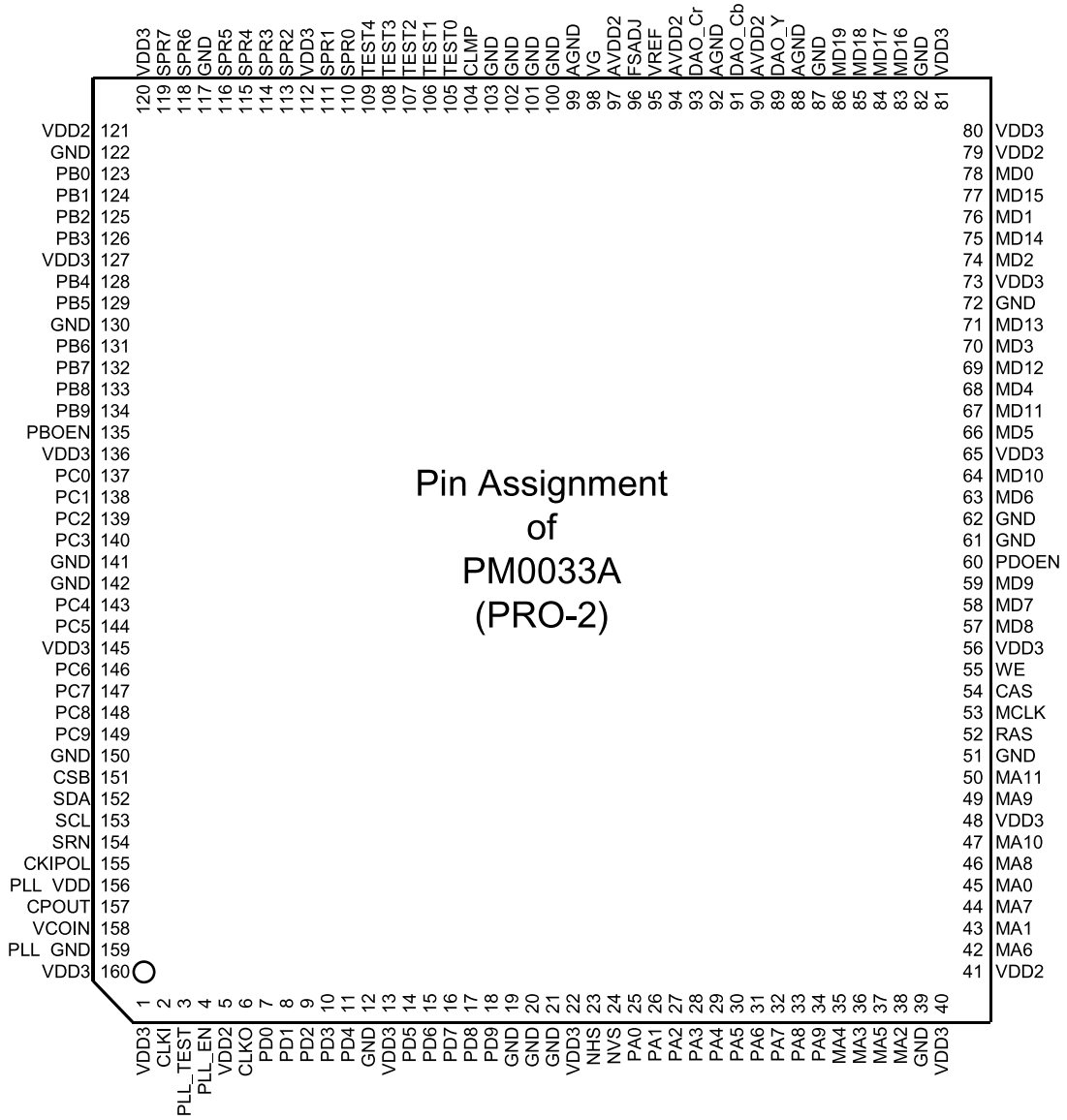
Pin Mnemonic	Input/Output	Function
DGND	G	Digital Ground
AGND	G	Analog Ground
GND_IO	G	Digital Ground
CLKIN_B	I	P xel Clock Input. Requires a 27MHz reference clock for Progressive Scan Mode or a 74.25MHz (74.1758MHz) reference clock in HDTV mode. This clock input pin is only used in simultaneous SD and HD mode.
CLKIN_A	I	P xel Clock Input for HD only or SD only modes.
COMP	O	Compensation Pin for DACs. Connect 0.1µF Capacitor from COMP pin to V_{AA}.
DAC A	O	CVBS/ GREEN/ Y SD analog output.
DAC B	O	Luma/ BLUE/ U SD analog output.
DAC C	O	Chroma/ RED/ V SD analog output.
DAC D	O	in SD only mode: CVBS/GREEN/ Y analog output in HD only mode and simultaneous HD/SD : Y/ GREEN (HD) analog output.
DAC E	O	in SD only mode: Luma/BLUE/ U analog output in HD only mode and simultaneous HD/SD : Pr/ RED (HD) analog output.
DAC F	O	in SD only mode: Chroma/RED/ V analog output in HD only mode and simultaneous HD/SD : Pb/ BLUE (HD) analog output.
P_BLANK	I	Video Blanking Control Signal for HD sync in simultaneous SD/HD mode and HD HD only mode.
$\overline{P}$_$\overline{HSYNC}$	I	Video Horizontal Sync Control Signal for HD sync in simultaneous SD/HD mode and HD only mode.
$\overline{P}$_$\overline{VSYNC}$	I	Video Vertical Sync Control Signal for HD sync in simultaneous SD/HD mode and HD only mode.
$\overline{S}$_$\overline{BLANK}$	I/O	Video Blanking Control Signal for SD.
$\overline{S}$_$\overline{HSYNC}$	I/O	Video Horizontal Control Signal for SD. Option to o/p SD HSYNC or HD HSYNC in SD Slave Mode 0 and/or any HD mode.
$\overline{S}$_$\overline{VSYNC}$	I/O	Video Blanking Control Signal for SD. Option to o/p SD VSYNC or SD HSYNC in SD Slave Mode 0 and/or any HD mode.
C9-0	I	10-Bit Progressive scan/ HDTV input port for CrCb color data in 4:2:2 input mode. In 4:4:4 input mode this input port is used for the Cb [Blue/U] data. The LSBs are set up on pins C0, C1. In default mode the input on this port is output on DAC E.
Y9-0	I	10-Bit Progressive scan/ HDTV input port for Y data. The LSBs are set up on pins Y0, Y1. In default mode the input on this port is output on DAC D.
S9-S0	I	10-Bit Standard Definition input port. Or Progressive Scan/ HDTV input port for Cr [Red/V] color data in 4:4:4 input mode. The LSBs are set up on pins S0, S1. In default mode the input on this port is output on DAC F.
$\overline{RESET}$	I	This input resets the on-chip timing generator and sets the ADV7300/01 into Default Register setting. Reset is an active low signal.

$R_{SET1,2}$	I	A 1520 Ohms resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
SCL_SI	I	Multifunctional input: MPU Port Serial Interface Clock Input or SPI input.
SDA_CLKSP	I/O	Multifunctional pin: MPU Port Serial Data Input/Output or SPI clock input.
ALSB_SO	I/O	Multifunctional pin. TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied low the I2C filter is activated which reduces noise on the I2C interface. When this pin is tied high, the input bandwidth on the I2C lines is increased. SPI output.
$\overline{SPI}$/I2C	I	When this nput pin is brought low, the ADV7300/01 interfaces over the SPI port and uses this input as part of the 4 wire SPI nterface. When this input pin is tied high [Vdd_IO], the ADV7300/01 interfaces over the I2C port.
V_{DD_IO}	P	Digital power supply
V_{DD}	P	Digital power supply
V_{AA}	P	Analog power supply
V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235V).
EXT_LF	I	External Loop filter for the internal PLL.
RTC_SCR_TR	I	Multifunctional Input: Real Time Control (RTC) nput, Timing Reset nput, Subcarrier Reset nput.

■ PM0033A (DVDM ASSY : IC902)

• Progressive Scan Converter (PRO2)

● Pin Arrangement



● **Pin Function**

Pin No.	Name	I/O/ P	Attribute	Functional Description
1	VDD3	P	-	VDD for IO (3.3V)
2	CLKI	In	LVTTL	27MHz System clock input terminal
3	PLL_TEST	In	LVTTL	Test exclusive use input terminal
4	PLL_EN	In	LVTTL	PLL enable input terminal
5	VDD2	P	-	VDD for Core (2.5V)
6	CLKO	Out	2mA	27MHz Clock output terminal
7	PD0	Inout	LVTTL, leakage, 2mA	Image data I/O port D(LSB)
8	PD1	Inout	LVTTL, leakage, 2mA	Image data I/O port D
9	PD2	Inout	LVTTL, leakage, 2mA	Image data I/O port D
10	PD3	Inout	LVTTL, leakage, 2mA	Image data I/O port D
11	PD4	Inout	LVTTL, leakage, 2mA	Image data I/O port D
12	GND	P	-	Digital Ground
13	VDD3	P	-	VDD for IO (3.3V)
14	PD5	Inout	LVTTL, leakage, 2mA	Image data I/O port D
15	PD6	Inout	LVTTL, leakage, 2mA	Image data I/O port D
16	PD7	Inout	LVTTL, leakage, 2mA	Image data I/O port D
17	PD8	Inout	LVTTL, leakage, 2mA	Image data I/O port D
18	PD9	Inout	LVTTL, leakage, 2mA	Image data I/O port D(MSB)
19	GND	P	-	Digital Ground
20	GND	P	-	Digital Ground
21	GND	P	-	Digital Ground
22	VDD3	P	-	VDD for IO (3.3V)
23	NHS	In	Schmitt	Horizontal synchronization input terminal
24	NVS	In	Schmitt	Vertical synchronization input terminal
25	PA0	In	LVTTL	Image data I/O port A(LSB)
26	PA1	In	LVTTL	Image data I/O port A
27	PA2	In	LVTTL	Image data I/O port A
28	PA3	In	LVTTL	Image data I/O port A
29	PA4	In	LVTTL	Image data I/O port A
30	PA5	In	LVTTL	Image data I/O port A
31	PA6	In	LVTTL	Image data I/O port A
32	PA7	In	LVTTL	Image data I/O port A
33	PA8	In	LVTTL	Image data I/O port A
34	PA9	In	LVTTL	Image data I/O port A(MSB)
35	MA4	Out	2mA	SDRAM address output terminal
36	MA3	Out	2mA	SDRAM address output terminal
37	MA5	Out	2mA	SDRAM address output terminal
38	MA2	Out	2mA	SDRAM address output terminal
39	GND	P	-	Digital Ground
40	VDD3	P	-	VDD for IO (3.3V)

Pin No.	Name	I/O/ P	Attribute	Functional Description
41	VDD2	P	-	VDD for Core (2.5V)
42	MA6	Out	2mA	SDRAM address output terminal
43	MA1	Out	2mA	SDRAM address output terminal
44	MA7	Out	2mA	SDRAM address output terminal
45	MA0	Out	2mA	SDRAM address output terminal(LSB)
46	MA8	Out	2mA	SDRAM address output terminal
47	MA10	Out	2mA	SDRAM address output terminal
48	VDD3	P	-	VDD for IO (3.3V)
49	MA9	Out	2mA	SDRAM address output terminal
50	MA11	Out	2mA	SDRAM address output terminal(MSB)
51	GND	P	-	Digital Ground
52	RAS	Out	2mA	SDRAM Row Address Strobe Command output terminal
53	MCLK	Out	4mA	SDRAM Clock output terminal (54MHz)
54	CAS	Out	2mA	SDRAM Column Address Strobe Command output terminal
55	WE	Out	2mA	SDRAM Write Enable output terminal
56	VDD3	P	-	VDD for IO (3.3V)
57	MD8	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
58	MD7	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
59	MD9	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
60	PDOEN	In	LVTTL	Image port D input and output setting input terminal (L: input, H: output)
61	GND	P	-	Digital Ground
62	GND	P	-	Digital Ground
63	MD6	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
64	MD10	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
65	VDD3	P	-	VDD for IO (3.3V)
66	MD5	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
67	MD11	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
68	MD4	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
69	MD12	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
70	MD3	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
71	MD13	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
72	GND	P	-	Digital Ground
73	VDD3	P	-	VDD for IO (3.3V)
74	MD2	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
75	MD14	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
76	MD1	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
77	MD15	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
78	MD0	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal(LSB)
79	VDD2	P	-	VDD for Core (2.5V)
80	VDD3	P	-	VDD for IO (3.3V)
81	VDD3	P	-	VDD for IO (3.3V)
82	GND	P	-	Digital Ground
83	MD16	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal

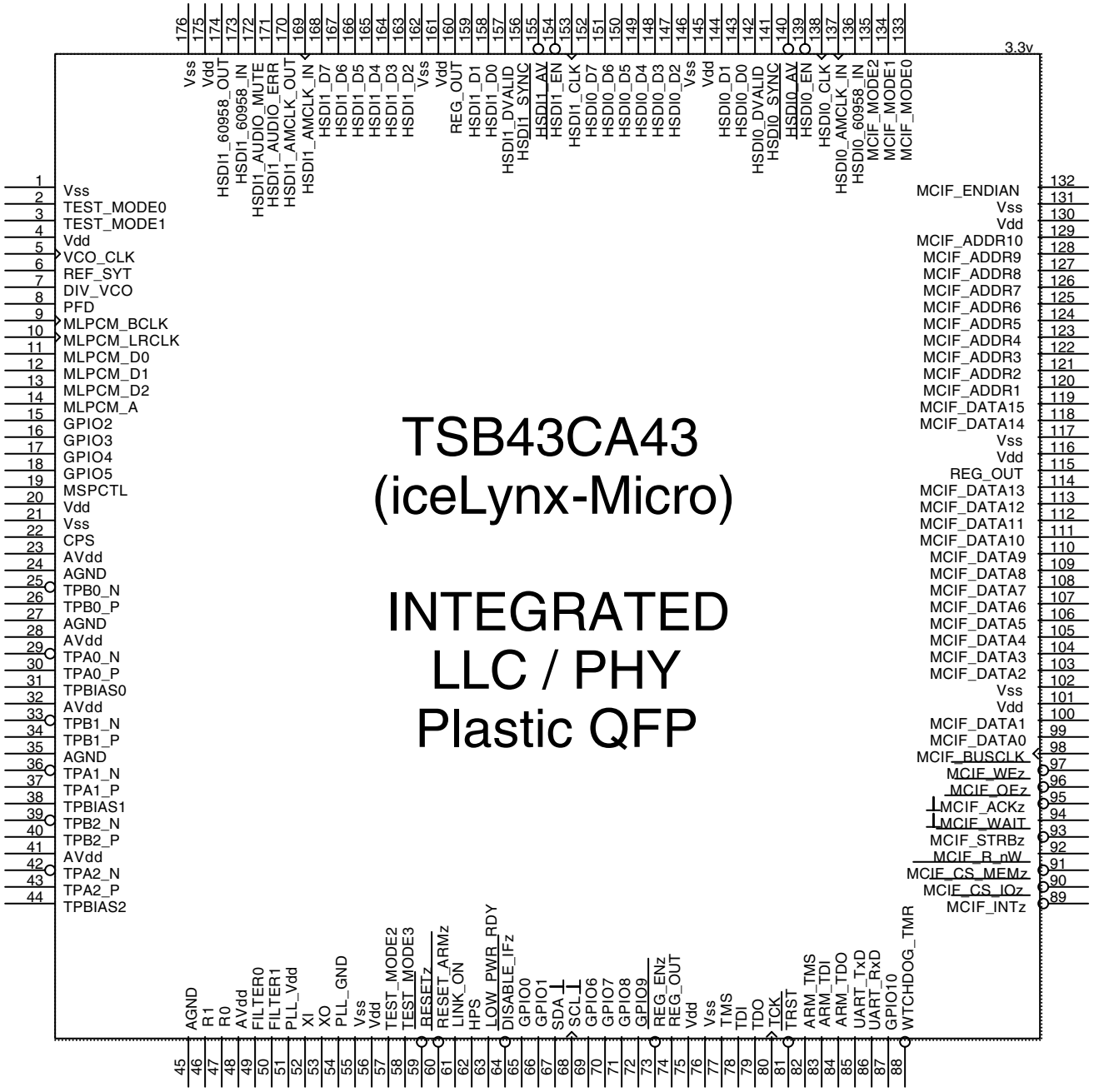
Pin No.	Name	I/O/ P	Attribute	Functional Description
84	MD17	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
85	MD18	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal
86	MD19	Inout	LVTTL, 2mA, Pullup	SDRAM data input-output terminal(MSB)
87	GND	P	-	Digital Ground
88	AGND	P	-	Ground for DAC
89	DAO_Y	Out	-	Analog video-out (Y)
90	AVDD2	P	-	VDD for DAC (2.5V)
91	DAO_Cb	Out	-	Analog video-out (Cb)
92	AGND	P	-	Ground for DAC
93	DAO_Cr	Out	-	Analog video-out (Cr)
94	AVDD2	P	-	VDD for DAC (2.5V)
95	VREF	In	-	DAC reference voltage input terminal
96	FSADJ	Inout	-	An ohms connection terminal for DAC peak swing setting
97	AVDD2	P	-	VDD for DAC (2.5V)
98	VG	Out	-	A volume connection terminal for gate voltage compensation of a DAC electric current cell
99	AGND	P	-	Ground for DAC
100	GND	P	-	Digital Ground
101	GND	P	-	Digital Ground
102	GND	P	-	Digital Ground
103	GND	P	-	Digital Ground
104	CLMP	Out	2mA	Clamp pulse output terminal
105	TEST0	In	LVTTL	Test exclusive use input terminal
106	TEST1	In	LVTTL	Test exclusive use input terminal
107	TEST2	In	LVTTL	Test exclusive use input terminal
108	TEST3	In	LVTTL	Test exclusive use input terminal
109	TEST4	In	LVTTL	Test exclusive use input terminal
110	SPR0	Out	2mA	Serial-to-parallel conversion output terminal(LSB)
111	SPR1	Out	2mA	Serial-to-parallel conversion output terminal
112	VDD3	P	-	VDD for IO (3.3V)
113	SPR2	Out	2mA	Serial-to-parallel conversion output terminal
114	SPR3	Out	2mA	Serial-to-parallel conversion output terminal
115	SPR4	Out	2mA	Serial-to-parallel conversion output terminal
116	SPR5	Out	2mA	Serial-to-parallel conversion output terminal
117	GND	P	-	Digital Ground
118	SPR6	Out	2mA	Serial-to-parallel conversion output terminal
119	SPR7	Out	2mA	Serial-to-parallel conversion output terminal(MSB)
120	VDD3	P	-	VDD for IO (3.3V)
121	VDD2	P	-	VDD for Core (2.5V)
122	GND	P	-	Digital Ground
123	PB0	Inout	LVTTL, leakage, 2mA	Image data I/O port B(LSB)
124	PB1	Inout	LVTTL, leakage, 2mA	Image data I/O port B
125	PB2	Inout	LVTTL, leakage, 2mA	Image data I/O port B
126	PB3	Inout	LVTTL, leakage, 2mA	Image data I/O port B
127	VDD3	P	-	VDD for IO (3.3V)
128	PB4	Inout	LVTTL, leakage, 2mA	Image data I/O port B

Pin No.	Name	I/O/ P	Attribute	Functional Description
129	PB5	Inout	LVTTL, leakage, 2mA	Image data I/O port B
130	GND	P	-	Digital Ground
131	PB6	Inout	LVTTL, leakage, 2mA	Image data I/O port B
132	PB7	Inout	LVTTL, leakage, 2mA	Image data I/O port B
133	PB8	Inout	LVTTL, leakage, 2mA	Image data I/O port B
134	PB9	Inout	LVTTL, leakage, 2mA	Image data I/O port B(MSB)
135	PBOEN	In	LVTTL	Image port B input and output setting input terminal (L: input, H: output)
136	VDD3	P	-	VDD for IO (3.3V)
137	PC0	Out	2mA	Image data I/O port C(LSB)
138	PC1	Out	2mA	Image data I/O port C
139	PC2	Out	2mA	Image data I/O port C
140	PC3	Out	2mA	Image data I/O port C
141	GND	P	-	Digital Ground
142	GND	P	-	Digital Ground
143	PC4	Out	2mA	Image data I/O port C
144	PC5	Out	2mA	Image data I/O port C
145	VDD3	P	-	VDD for IO (3.3V)
146	PC6	Out	2mA	Image data I/O port C
147	PC7	Out	2mA	Image data I/O port C
148	PC8	Out	2mA	Image data I/O port C
149	PC9	Out	2mA	Image data I/O port C(MSB)
150	GND	P	-	Digital Ground
151	CSB	In	Schmitt	MPU Interface chip select input terminal
152	SDA	In	Schmitt	MPU Interface data entry terminal
153	SCL	In	Schmitt	MPU Interface clock input terminal
154	SRN	In	Schmitt	System reset input terminal
155	CKIPOL	In	LVTTL	System clock polarity setting input terminal
156	PLL_VDD	P	-	VDD of PLL exclusive use (2.5V)
157	CPOUT	Out	Analog	Analog output terminal from PLL charge pump
158	VCOIN	In	Analog	Analog input terminal from PLL outside charge account loop filter
159	PLL_GND	P	-	Ground of PLL exclusive use
160	VDD3	P	-	VDD for IO (3.3V)

■ TSB43CA43GGW (ILKB ASSY : IC201)

• IEEE1394 PHY LINK

● Pin Arrangement



● **Pin Function**

Pin Name	Pin No	I/O	Description
Power & Ground Pins			
DISABLE_IFZ	64	I	Interface Disable. When asserted, the interfaces are put into a Hi-Z state. Interfaces include: ex-CPU, HSDI, GPIO, and WTCH_DG_TMRZ.
HPS	62	I	Host Power Status. This indicates the power status of the external system to iceLynx-Micro. A rising edge indicates the system CPU has been turned ON. (The internal ARM should wake up.) A falling edge indicates the system CPU has been turned OFF. (The internal ARM decides if power down is necessary.)
LOW_PWR_RDY	63	O	Output to system to indicate iceLynx-Micro is ready to go into a low power state. The ARM and WTCH_DG_TMRZ control this pin.
WTCH_DG_TMRZ	88	O	Watch Dog Timer (for the ARM.) iceLynx-Micro hardware asserts this pin whenever ARM software has not updated the Timer2 register within the allowed time period.
RESET_ARMZ	60	I	ARM reset. This signal resets the internal ARM processor.
RESETZ	59	I/O	Device reset. This signal resets all logic. This includes the PHY, Link core, memory, the ARM, and random logic.
VSS	1, 21, 55, 76, 102 117 131, 146, 162 176		Digital Ground.
AGND	24, 27, 35, 45,		Analog Ground.
PLL_GND	54		PLL Ground.
VDD	4, 20, 56, 75, 101 116, 130 145, 161 175		Digital Power Supply. Must be set to 3.3V nominal.

Pin Name	Pin No	I/O	Description
AVDD	23, 28, 32, 41, 48		Analog Power Supply. Must be set to 3.3V nominal.
PLL_VDD	51		PLL Power Supply. Must be set to 3.3V nominal.
Regulator Pins			
REG_ENZ	73	I	Internal Regulator Enable. The iceLynx-Micro core voltage is 1.8V. Internal regulators are used to regulate the 3.3V VDD inputs to 1.8V. This pin enables the regulators.
REG_OUT0	74	O	1.8V Regulator Output. This pin should be connected to ground using a 0.1uF capacitor.
REG_OUT1	115	O	1.8V Regulator Output. This pin should be connected to ground using a 0.1uF capacitor.
REG_OUT2	160	O	1.8V Regulator Output. This pin should be connected to ground using a 0.1uF capacitor.
External CPU Interface Pins			
MCIF_ACKZ	95	I/O	MCIF Acknowledge pin. Default active low. iceLynx-Micro asserts this signal if it has completed the MCIF request. This signal is always driven. This signal is used for the following modes: • 68000 + Wait I/O Access • MPC850 I/O Access In Serial MCIF Mode, this pin is used for the Serial Read Acknowledge (SMCIF_RACKZ.)
MCIF_ADDR1	120	I	MCIF Address 1 pin. This data pin is the least significant bit of the MCIF Address Bus. MCIF_ADDR0 is internally grounded. Only 16-bit addressing is allowed. MCIF_ADDR1 should be connected to the Address1 signal of the system CPU.
MCIF_ADDR10	129	I	MCIF Address 10 pin. This data pin is the most significant bit of the MCIF Address Bus.
MCIF_ADDR2	121	I	MCIF Address 2 pin
MCIF_ADDR3	122	I	MCIF Address 3 pin
MCIF_ADDR4	123	I	MCIF Address 4 pin
MCIF_ADDR5	124	I	MCIF Address 5 pin
MCIF_ADDR6	125	I	MCIF Address 6 pin
MCIF_ADDR7	126	I	MCIF Address 7 pin
MCIF_ADDR8	127	I	MCIF Address 8 pin
MCIF_ADDR9	128	I	MCIF Address 9 pin

Pin Name	Pin No	I/O	Description
MCIF_BUSCLK	98	I	MCIF Bus Clock. This pin is only used for the MCIF synchronous mode. (MPC850 I/O Access) and the Memory Access. This signal should be tied high if not used. In Serial MCIF Mode, this pin is used for the Serial Write Clock (SMCIF_WCLK.)
MCIF_CS_IOZ	90	I	MCIF Chip Select for all I/O MCIF modes. In Serial MCIF Mode, this pin is used for the Serial Write Request (SMCIF_WREQZ.)
MCIF_CS_MEMZ	91	I/O	MCIF Chip Select for the Memory MCIF mode. In Serial MCIF Mode, this pin is used for the Serial Write Acknowledge (SMCIF_WACKZ.)
MCIF_DATA0	99	I/O	MCIF DATA 0 pin. This data pin is the least significant bit of the MCIF Data Bus. In Serial MCIF Mode, this pin is used for the Serial Read Data (SMCIF_RDATA.)
MCIF_DATA1	100	I/O	MCIF DATA 1 pin.
MCIF_DATA10	111	I/O	MCIF DATA 10 pin.
MCIF_DATA11	112	I/O	MCIF DATA 11 pin.
MCIF_DATA12	113	I/O	MCIF DATA 12 pin.
MCIF_DATA13	114	I/O	MCIF DATA 13 pin.
MCIF_DATA14	118	I/O	MCIF DATA 14 pin.
MCIF_DATA15	119	I/O	MCIF DATA 15 pin. This data pin is the most significant bit of the MCIF Data Bus.
MCIF_DATA2	103	I/O	MCIF DATA 2 pin.
MCIF_DATA3	104	I/O	MCIF DATA 3 pin.
MCIF_DATA4	105	I/O	MCIF DATA 4 pin.
MCIF_DATA5	106	I/O	MCIF DATA 5 pin.
MCIF_DATA6	107	I/O	MCIF DATA 6 pin.
MCIF_DATA7	108	I/O	MCIF DATA 7 pin.
MCIF_DATA8	109	I/O	MCIF DATA 8 pin.
MCIF_DATA9	110	I/O	MCIF DATA 9 pin.
MCIF_ENDIAN	132	I	MCIF Endian Pin. This sets the Endianess for accesses between the external CPU and the internal iceLynx-Micro memory. This pin sets Endianess for all MCIF modes and the Serial MCIF mode. When set to a logical 0, data is read/written to the ex-CPU exactly as it is stored in iceLynx-Micro memory. (Big Endian) When set to a logical 1, data is swapped on half-word and byte boundaries before it is read/written to the ex-CPU. (Little Endian)

Pin Name	Pin No	I/O	Description
MCIF_INTZ	89	O	MCIF Interrupt. This signal is push-pull. (always asserted) It does not require a pull-up resistor.
MCIF_MODE0	133	I	MCIF Mode 0. Used to select MCIF mode.
MCIF_MODE1	134	I	MCIF Mode 1. Used to select MCIF mode.
MCIF_MODE2	135	I	MCIF Mode 2. Used to select MCIF mode.
MCIF_OEZ	96	I	MCIF Output Enable. Default active low. This input pin indicates if the system CPU wants to perform a MCIF read access. This signal is used for the following modes: • SH-3 I/O Access • M16C/62 I/O Access • Memory Access This signal should be tied high if not used.
MCIF_RW	92	I	MCIF Read/Write pin. Default value for read is a logical 1. Default value for write is a logical 0. In Serial MCIF Mode, this pin is used for the Serial Write Data (SMCIF_WDATA.)
MCIF_STRBZ	93	I	MCIF Strobe pin. Default active low. This pin is used (along with MCIF_CS_IOZ) to validate the MCIF access. This signal is used for the following modes: • 68000 + Wait I/O Access • MPC850 I/O Access • When not used, this pin should be tied high. In Serial MCIF Mode, this pin is used for the Serial Read Clock (SMCIF_RCLK.)
MCIF_WAIT	94	O	MCIF Wait pin. Default active high. iceLynx-Micro asserts this signal if it is not ready to service an MCIF request. When not asserted, this signal is in high-Z state. This signal is used for the following modes: • 68000 + Wait I/O Access • SH-3 I/O Access • M16C/62 I/O Access In Serial MCIF Mode, this pin is used for the Serial Read Request (SMCIF_RREQZ.)
MCIF_WEZ	97	I	MCIF Write Enable. Default active low. This input pin indicates if the system CPU wants to perform a MCIF write access. This signal is used for the following modes: • SH-3 I/O Access • M16C/62 I/O Access • Memory Access This signal should be tied high if not used.
Universal Asynchronous Receiver Transmitter Pins			
UART_RxD	86	I	UART receive port. Data from the system is input to the UART buffer using this pin.
UART_TxD	85	O	UART transmit port. Data from the UART buffer is output to the system using this pin.

Pin Name	Pin No	I/O	Description
Joint Test Action Group (JTAG) & ARM Pins			
JTAG_TCK	80	I	JTAG Clock pin. Both the boundary scan and ARM JTAG uses this input for the JTAG clock.
JTAG_TDI	78	I	JTAG Test Data Input pin
JTAG_TDO	79	O	JTAG Test Data Output pin
JTAG_TMS	77	I	JTAG Test Mode Selector pin.
JTAG_TRST	81	I	JTAG Reset Pin. Both the boundary scan and ARM JTAG uses this input for the JTAG clock.
ARM_JTAG_TDI	83	I	ARM JTAG Test Data Input pin
ARM_JTAG_TDO	84	O	ARM JTAG Test Data Output pin
ARM_JTAG_TMS	82	I	ARM JTAG Test Mode Selector pin
I^2C Serial Bus Pins			
SCL	68	I/O	I^2C Clock Pin. This pin should be tied to ground if no EEPOM is used. For EEPROM write operations, the GPIO8 settings are muxed with the SCL pin. Software can manipulate the GPIO8 register settings in order to perform a write.
SDA	67	I/O	I^2C Data Pin For EEPROM write operations, the GPIO9 settings are muxed with the SDA pin. Software can manipulate the GPIO9 register settings in order to perform a write.
General Purpose Input/Out Pins (GPIO)			
GPIO0	65	I/O	GPIO0. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO1	66	I/O	GPIO1. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO2	15	I/O	GPIO2. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO3	16	I/O	GPIO3. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO4	17	I/O	GPIO 4. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO5	18	I/O	GPIO 5. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO6	69	I/O	GPIO6. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO7	70	I/O	GPIO7. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.

Pin Name		I/O	Description
GPIO8	71	I/O	GPIO8. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO9	72	I/O	GPIO9. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
GPIO10	87	I/O	GPIO10. Can be programmed as general-purpose input, general-purpose output, or specific function. Power-up default is input.
Physical Layer Pins			
TPA0_N TPA1_N TPA2_N TPA0_P TPA1_P TPA2_P	29 36 42 30 37 43	I/O	Twisted Pair A Differential Signal Terminals. For an unused port, TPAN and TPAP signals can be left open.
TPB0_N TPB1_N TPB2_N TPB0_P TPB1_P TPB2_P	25 33 39 26 34 40	I/O	Twisted Pair B Differential Signal Terminals. For an unused port, TPBN and TPBP signals can be left open.
TPBIAS0 TPBIAS1 TPBIAS2	31 38 44	I/O	Twisted Pair Bias Output. These signals provide the 1.86V nominal bias voltage needed for proper operation of the twisted pair driver and receivers for signaling an ìactive connectionî to a remote node. For an unused port, TPBIAS can be left unconnected.
R1 R0	46 47	-	Current Setting Resistors. These pins are connected to external resistors to set the internal operating currents and cable driver output currents. A resistance of 6.34kΩ ± 1% is required to meet the IEEE 1394-1995 output voltage limits.
FILTER0 FILTER1	49 50	I/O	PLL Filter Terminals. These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency-multiplier PLL, which is using the crystal oscillator. A 0.1 µF± 10% capacitor is the only external component required to complete this filter.
XI X0	52 53	-	Crystal Oscillator Inputs. These terminals connect to a 24.576 MHz parallel resonant fundamental mode crystal. The optimum values for the external shunt capacitors are dependent on the crystal used.
CPS	21	I	Cable Power Status. Input to iceLynx-Micro used to detect if cable power is present. This pin should be connected to the cable power through 390 kΩ resistor.
MSPCTL	19	I	
LINKON	61	O	Link On output. This signal is asserted whenever LPS is low and a Link On packet is received from the 1394 bus.
High Speed Data Interface (HSDI) Port 0 Pins			
HSDI_60958_IN	173	I	60958 Data Input.

Pin Name	Pin No	I/O	Description
HSDI_60958_OUT	179	O	60958 Data Output This signal is also used as FLWCTRL_DVALID in Flow Control Data Valid mode.
HSDI0_60958_IN	136	I	60958 Data Input.
HSDI0_AMCLK_IN	137	I	Audio Master Clock Input. This clock is used to decode the bi-phase encoding of 60958 data. This pin is also used to input the 1.5*BCLK for Flow Control mode.
HSDI0_AV	140	O	HSDI Port 0 Available. Programmable. Default active low. For receive from 1394, this signal indicates if a 1394 packet is available in the receive buffer for reading. The HSDI_AV signal for MPEG2 data also depends on time stamp based release. For transmit onto 1394, this signal can be used to indicate buffer level in HSDI TX mode 8 and 9 by programming a CFR. If the buffer level is above a programmed level, HSDI_AV will be asserted.
HSDI0_CLK	138	I	HSDI Port 0 Clock. Programmable. Default rising edge sample. This clock is used to operate the HSDI port 0 logic. In parallel mode, the maximum clock is 27MHz. In serial mode, the maximum clock is 70MHz. This signal is output to HSDI1_CLK in pass thru mode. This signal can be used as HSDI0_MLPCM_BCLK for DVD-Audio Transmit.
HSDI0_D0	143	I/O	HSDI Port 0 Data 0 Pin. Data 0 is the least significant bit on the HSDI data bus. In serial mode, only HSDI0_D0 is used. This signal is output to HSDI1_D0 in pass thru mode. This signal can be used as HSDI0_MLPCM_D0 for DVD-Audio Transmit.
HSDI0_D1	144	I/O	HSDI Port 0 Data 1 Pin This signal is output to HSDI1_D1 in pass thru mode. This signal can be used as HSDI0_MLPCM_D1 for DVD-Audio Transmit.
HSDI0_D2	147	I/O	HSDI Port 0 Data 2 Pin This signal is output to HSDI1_D2 in pass thru mode. This signal can be used as HSDI0_MLPCM_D2 for DVD-Audio Transmit.
HSDI0_D3	148	I/O	HSDI Port 0 Data 3 Pin This signal is output to HSDI1_D3 in pass thru mode. This signal can be used as HSDI0_MLPCM_A for DVD-Audio Transmit.
HSDI0_D4	149	I/O	HSDI Port 0 Data 4 Pin This signal is output to HSDI1_D4 in pass thru mode

Pin Name	Pin No	I/O	Description
HSDI0_D5	150	I/O	HSDI Port 0 Data 5 Pin This signal is output to HSDI1_D5 in pass thru mode
HSDI0_D6	151	I/O	HSDI Port 0 Data 6 Pin This signal is output to HSDI1_D6 in pass thru mode
HSDI0_D7	152	I/O	HSDI Port 0 Data 7 Pin. Data 0 is the most significant bit on the HSDI data bus. This signal is output to HSDI1_D7 in pass thru mode
HSDI0_DVALID	142	I/O	HSDI Port 0 Data Valid Pin. Programmable. Default active high. This pin indicates if data on the HSDI data bus valid for reading or writing. For transmit onto 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. For HSDI DV modes, this signal is used as HSDI0_FrameSync indicating DV frame boundary. This signal is output to HSDI1_DVALID in pass thru mode If not used in transmit mode, this signal can be tied low.
HSDI0_EN	139	I	HSDI Port 0 Enable. Programmable. Default active low. Input by the system to enable the HSDI for both transmit and receive from 1394. If not used, this signal can be tied enabled (low or high depending on the polarity set). The application can use HSDI_DVALID or HSDI_SYNC to validate the HSDI data. This signal can be used as HSDI0_MLPCM_LRCLK for DVD-Audio Transmit.
HSDI0_SYNC	141	I/O	HSDI Port 0 Sync Signal. Programmable. Default active high. This signal is used to indicate the start of packet. For transmit onto 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. This signal is output to HSDI1_SYNC in pass thru mode. If not used in transmit mode, this signal can be tied low or high depending on the polarity.
High Speed Data Interface (HSDI) Port 1 Pins			

Pin Name	Pin No	I/O	Description
HSDI1_AMCLK_IN	169	I	Audio Master Clock Input. This clock is used to decode the bi-phase encoding of 60958 data. This pin is also used to input the 1.5*BCK for Flow Control mode. MLPCM Interface, HSDI1 Audio Port, and HSDI1 video port share buffer 1. Only one interface can access the buffer at a time.
HSDI1_AMCLK_OUT	170	O	Audio Master Clock Output. This clock is derived from the VCO_CLK input. 60958 data output from iceLynx-Micro is bi-phase encoded using this clock.
HSDI1_AUDIO_ERR	171	O	Audio Error Signal. iceLynx-Micro asserts this signal whenever an Audio Error condition occurs. (Receive from 1394 only.)
HSDI1_AUDIO_MUTE	172	O	Audio Mute Status. iceLynx-Micro asserts this signal whenever an Audio Mute condition has occurred, and hardware has muted the HSDI1 audio interface. (Receive from 1394 only.)
HSDI1_AV	155	O	HSDI Port 1 Available. Programmable. Default active low. For receive from 1394, this signal indicates if a 1394 packet is available in the receive buffer for reading. The HSDI_AV signal for MPEG2 data also depends on time stamp based release. For transmit onto 1394, this signal can be used to indicate buffer level in HSDI TX mode 8 and 9 by programming a CFR. This pin can be used to indicate buffer level in transmit mode by programming a CFR. If the buffer level is above a programmed level, HSDI_AV is asserted.
HSDI1_CLK	153	I/O	HSDI Port 1 Clock. Programmable. Default rising edge sample. This clock is used to operate the HSDI port 1 logic. In parallel mode, the maximum clock is 27MHz. In serial mode, the maximum clock is 70MHz. This signal can be used as HSDI1_SACD_MCLK for SACD Transmit and Receive. MLPCM Interface, HSDI1 Audio Port, and HSDI1 video port share buffer 1. Only one interface can access the buffer at a time.
HSDI1_D0	158	I/O	HSDI Port 1 Data 0 Pin. Data 0 is the least significant bit on the HSDI data bus. In serial mode, only HSDI0_D0 is used. This signal can be used as HSDI1_SACD_D0 for SACD Transmit and Receive.

Pin Name	Pin No	I/O	Description
HSDI1_D1	159	I/O	HSDI Port 1 Data 1 Pin This signal can be used as HSDI1_SACD_D1 for SACD Transmit and Receive.
HSDI1_D2	163	I/O	HSDI Port 1 Data 2 Pin This signal can be used as HSDI1_SACD_D2 for SACD Transmit and Receive.
HSDI1_D3	164	I/O	HSDI Port 1 Data 3 Pin This signal can be used as HSDI1_SACD_D3 for SACD Transmit and Receive.
HSDI1_D4	165	I/O	HSDI Port 1 Data 4 Pin This signal can be used as HSDI1_SACD_D4 for SACD Transmit and Receive.
HSDI1_D5	166	I/O	HSDI Port 1 Data 5 Pin This signal can be used as HSDI1_SACD_D5 for SACD Transmit and Receive.
HSDI1_D6	167	I/O	HSDI Port 1 Data 6 Pin This signal can be used as HSDI1_SACD_A for SACD Transmit and Receive.
HSDI1_D7	168	I/O	HSDI Port 1 Data 7 Pin. Data 0 is the most significant bit on the HSDI data bus.
HSDI1_DVALID	157	I/O	HSDI Port 1 Data Valid Pin. Programmable. Default active high. This pin indicates if data on the HSDI data bus valid for reading or writing. For transmit onto 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. For HSDI DV modes, this signal is used as HSDI0_FrameSync indicating DV frame boundary. If not used in transmit mode, this signal can be tied low.
HSDI1_EN	154	I	HSDI Port 1 Enable. Programmable. Default active low. Input by the system to enable the HSDI for both transmit and receive from 1394. If not used, this signal can be tied enabled (low or high depending on the polarity set). The application can use HSDI_DVALID or HSDI_SYNC to validate the HSDI data.

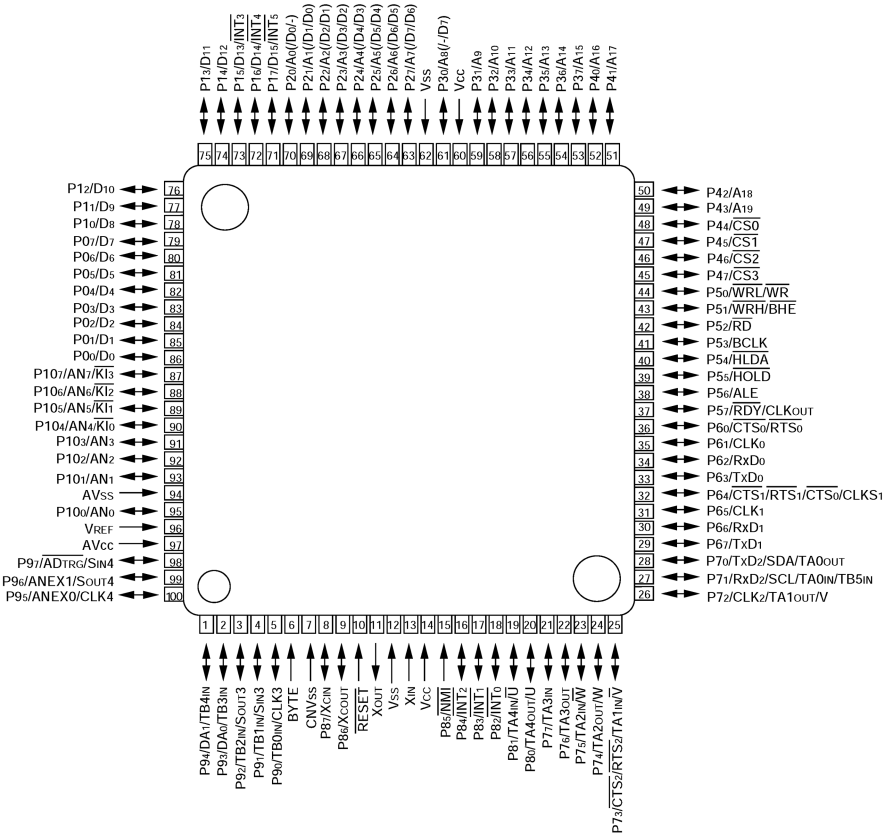
Pin Name	Pin No	I/O	Description
HSDI1_SYNC	156	I/O	HSDI Port 1 Sync Signal. Programmable. Default active high. This signal is used to indicate the start of packet For transmit onto 1394, this signal is provided by the system with the data. For receive from 1394, iceLynx-Micro provides this signal with the data. If not used in transmit mode, this signal can be tied low or high depending on the polarity. This signal can be used as HSDI1_SACD_FRAME for SACD Transmit and Receive.
DVD-Audio Interface Pins			
MLPCM_A	14	I/O	Audio MLPCM Interface Ancillary Data. Ancillary data is input/output using this pin. For DVD-Audio, MLPCM_LRCLK determines if Ancillary Left or Ancillary Right data is present. This signal also functions as FLWCTL_A in Flow Control mode
MLPCM_BCLK	9	I/O	Audio MLPCM Interface Bit Clock. Multiple functions: • DVD Audio BCK (I) • DVD Audio BCK (O) • Flow Control BCK (I/O) MLPCM Interface, HSDI1 Audio Port, and HSDI1 video port share buffer 1. Only one interface can access the buffer at a time.
MLPCM_D0	11	I/O	Audio MLPCM Interface D0. Contains Channel 1 and Channel 2 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in Flow Control mode.
MLPCM_D1	12	I/O	Audio MLPCM Interface D1. Contains Channel 3 and Channel 4 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in Flow Control mode
MLPCM_D2	13	I/O	Audio MLPCM Interface D2. Contains Channel 5 and Channel 6 information. MLPCM_LRCLK determines which channel is present. This signal also functions as FLWCTL_D0 in Flow Control mode
MLPCM_LRCLK	10	I/O	Audio MLPCM Interface Left-Right Clock. Multiple functions: DVD Audio LRCLK (I) DVD Audio LRCLK (O) Flow Control LRCLK (I/O)

Pin Name	Pin No	I/O	Description
Phase Lock Loops Pins			
DIV_VCO	7	O	Output for External Phase Detector. This signal is the divided VCO_CLK. It used by the external phase detector to compare with the REF_SYT signal. The divide ratios are setup in CFR.
PFD	8	O	Output from Internal Phase Detector. This signal can feed directly into the LPF and VCO if the internal phase detector is used.
REF_SYT	6	O	Output for External Phase Detector. This signal represents the SYT match for received audio or DV packets. The phase detector uses it as input to detect differences between the SYT match and the VCO clock.
VCO_CLK	5	I	Input from VCO. This is used to generate internal audio and DV clocks for receive clock recovery. Audio Frequency: 33.868MHz or 36.864MHz. DV Frequency: 30.72MHz
Test Mode Pins			
TEST_MODE0	2	I/O	Test Mode. Used for Internal TI testing. Should be tied low for normal operation.
TEST_MODE1	3	I/O	Test Mode. Used for Internal TI testing. Should be tied low for normal operation.
TEST_MODE2 TEST_MODE3	57 58	I/O	Test Mode. Used for Internal TI testing. Should be tied low for normal operation.

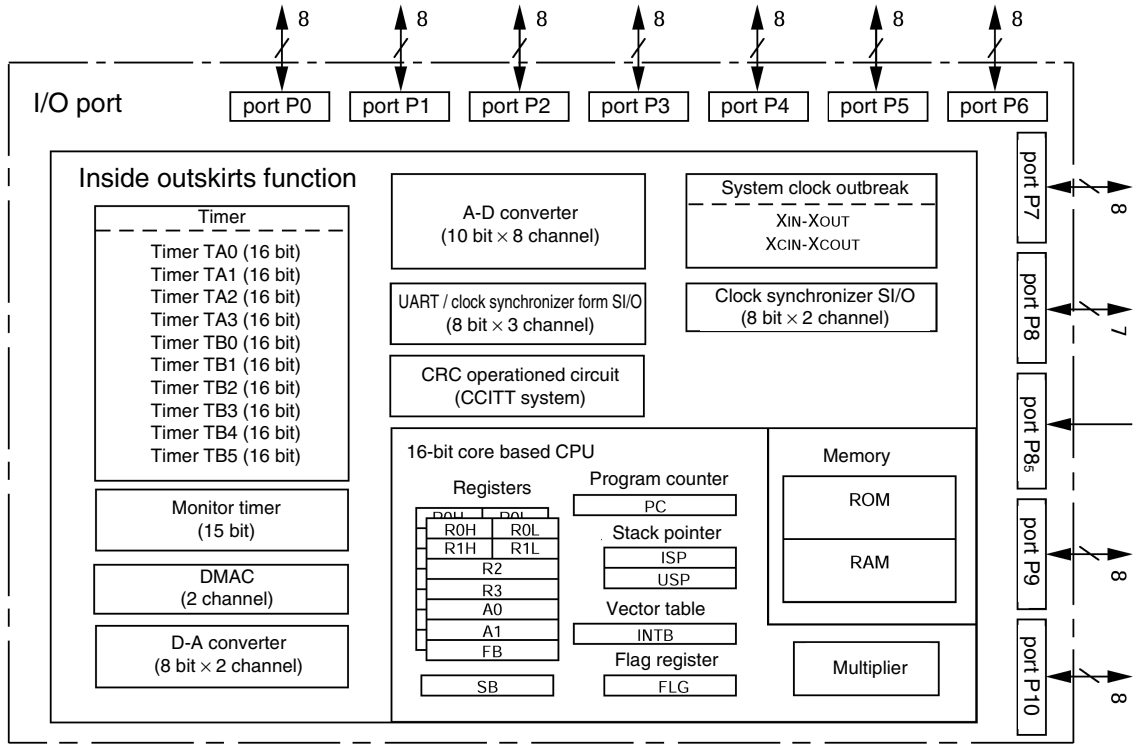
■ PD5787A (ILKB ASSY : IC101)

• HOST CPU

● Pin Arrangement



● Block Diagram



7.3 DISC / CONTENT FORMAT PLAYBACK COMPATIBILITY

Disc / Content Format Playback Compatibility

General Disc Compatibility

- This player was designed and engineered to be compatible with software bearing one or more of the following logos.

DVD-Audio DVD-Video DVD-R DVD-RW

Audio CD Video CD CD-R CD-RW

Super Audio CD

- Other formats, including but not limited to the following, are not playable in this player:

  Photo CD, DVD-RAM, DVD-ROM, CD-ROM

- DVD-R/RW and CD-R/RW discs (Audio CDs and Video CDs) recorded using a DVD recorder, CD recorder or personal computer may not be playable on this machine. This may be caused by a number of possibilities, including but not limited to: the type of disc used; the type of recording; damage, dirt or condensation on either the disc or the player s pick-up lens. See below for notes about particular software and formats.

CD-R/RW Compatibility

- This unit will play CD-R and CD-RW discs recorded in CD Audio or Video CD format, or as a CD-ROM containing MP3 audio files. However, any other content may cause the disc not to play, or create noise/distortion in the output.
- This unit cannot record CD-R or CD-RW discs.
- Unfinalized CD-R/RW discs recorded as CD Audio can be played, but the full Table of Contents (playing time, etc.) will not be displayed.

DVD-R/RW Compatibility

- This unit will play DVD-R/RW discs that were recorded using the DVD Video format or Video Recording format.
- This unit cannot record DVD-R/RW discs.
- Unfinalized DVD-R/RW discs cannot be played in this player.

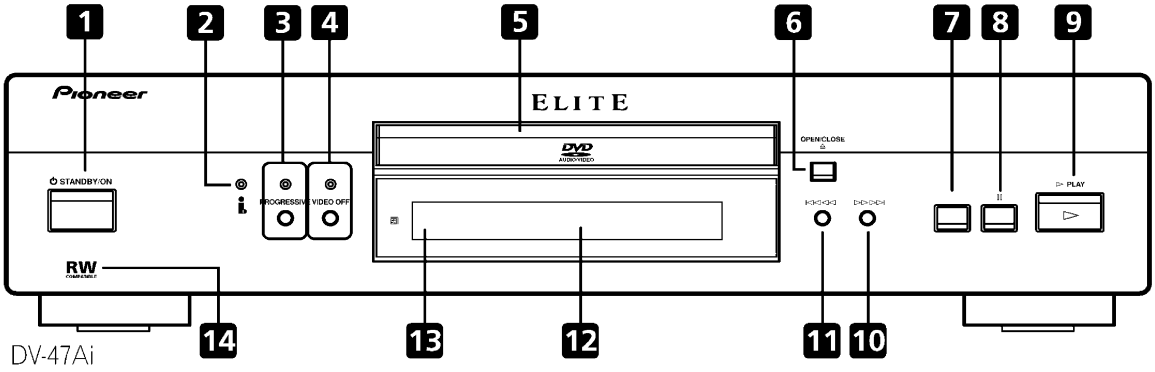
7.4 CLEANING

Before shipping out the product, be sure to clean the following positions by using the prescribed cleaning tools:

Position to be cleaned	Cleaning tools
Pickup lenses	Cleaning liquid : GEM1004 Cleaning paper : GED-008

8. PANEL FACILITIES

Front panel



DV-47Ai

1 ⏻ STANDBY/ON
DV-47Ai: Press to switch the player on or into standby

2 i.LINK indicator
Lights when audio is being sent over the i.LINK interface to a compatible component.

3 PROGRESSIVE button/indicator
Press to switch the progressive video output mode between progressive and interlace. The indicator lights in progressive scan mode.

4 VIDEO OFF button/indicator
Press to switch the video output on/off. The indicator lights when the video output is switched off (when listening to a DVD-Audio disc, for example)

5 Disc tray

6 ⏏ OPEN/CLOSE
Press to open or close the disc tray (when in standby, this button will also switch the power on)

7 ■ (stop)
Press to stop the disc (you can resume playback by pressing ► (play))

8 ❚❚ (pause)
Press to pause playback. Press again to restart

9 ► (play)
Press to start or resume playback (when in standby, this button will also switch the power on)

10 ►► ►►| (forward scan/skip)
- Press and hold for fast forward scanning
- Press to jump to the next chapter or track

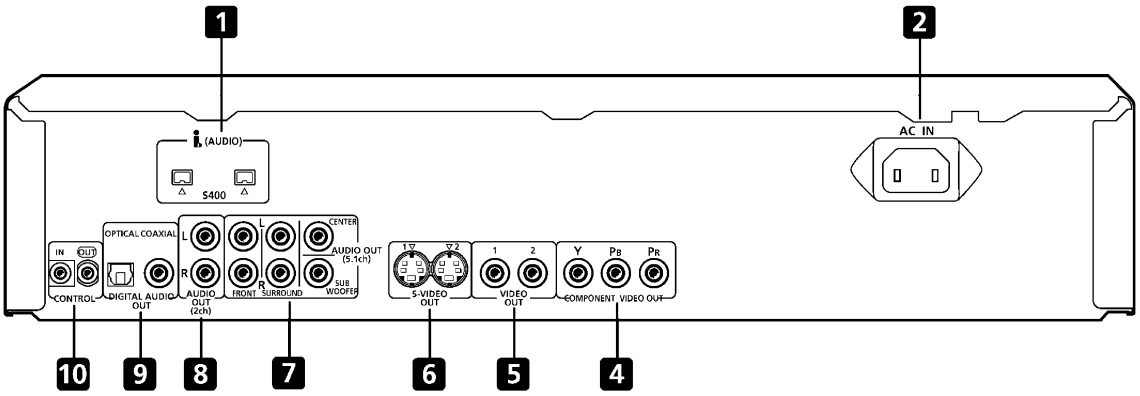
11 |◄◄ ◄◄ (reverse scan/skip)
- Press and hold for fast reverse scanning
- Press to jump back to the beginning of the current chapter or track, then to previous chapters/tracks

12 Display

13 Remote control sensor
The remote control has a range of up to about 23ft. (7m)

14 RW COMPATIBLE
This mark indicates compatibility with DVD-RW discs recorded on a DVD recorder in Video Recording mode.

Rear panel



DV-47Ai

When connecting this player up to your TV, AV receiver or other components, make sure that all components are switched off and unplugged.

1 i.LINK (AUDIO) – i.LINK connectors

4-pin, S400 i.LINK connectors for connection to i.LINK-equipped receivers and other components. Each i.LINK connector acts simultaneously as both input and output.

2 AC IN

Connect the supplied power cord here, then plug into a power outlet.

4 COMPONENT VIDEO OUT

High quality video output for connection to a TV, monitor or AV receiver that has component video inputs.

Connect using a commercially available three-way component video cable. Be careful to match the colors of the jacks and cables for correct connection.

5 VIDEO OUT (1&2)

Standard video output(s) that you can connect to your TV or AV receiver using the supplied audio/video cable.

6 S-VIDEO OUT (1&2)

S-Video output(s) that you can use instead of the **VIDEO OUT** jacks.

7 AUDIO OUT (5.1ch)

Multichannel analog audio outputs for connection to an AV receiver with multichannel inputs.

8 AUDIO OUT (2ch)

Two channel analog audio outputs for connection to your TV, AV receiver or stereo system.

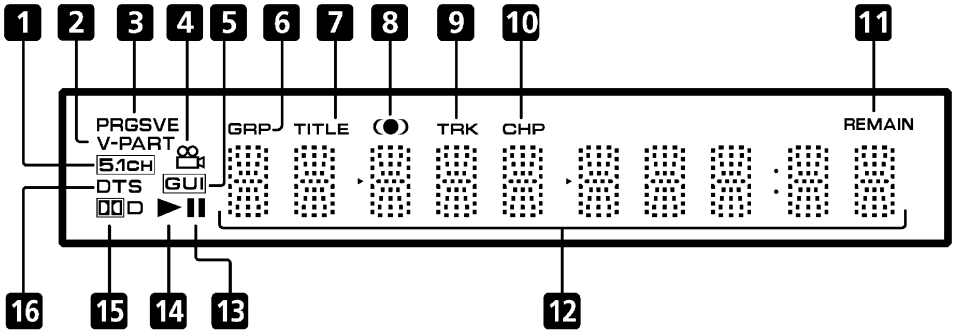
9 DIGITAL AUDIO OUT – OPTICAL / COAXIAL

Digital audio outputs for connection to a PCM, Dolby Digital, DTS and/or MPEG-compatible AV receiver.

10 CONTROL IN / OUT

For passing remote control signals to other Pioneer components.

Display



1 5.1CH
Lights when analog 5.1 channel output is selected

2 V-PART
Lights when playing a video part of a DVD disc

3 PRGSVE
Lights when the video output is progressive scan

4
Lights during multi-angle scenes on a DVD disc

5 GUI (Graphical User Interface)
Lights when a menu is displayed on-screen

6 GRP
Indicates that the character display is showing a DVD-Audio group number

7 TITLE
Indicates that the character display is showing a DVD-Video title number

8
Lights when V/TruSurround is active

9 TRK
Indicates that the character display is showing a track number

10 CHP
Indicates that the character display is showing a DVD chapter number

11 REMAIN
Lights when the character display is showing the time or number of tracks/titles/chapters remaining

12 Character display

13 ❚❚
Lights when a disc is paused

14 ►
Lights when a disc is playing

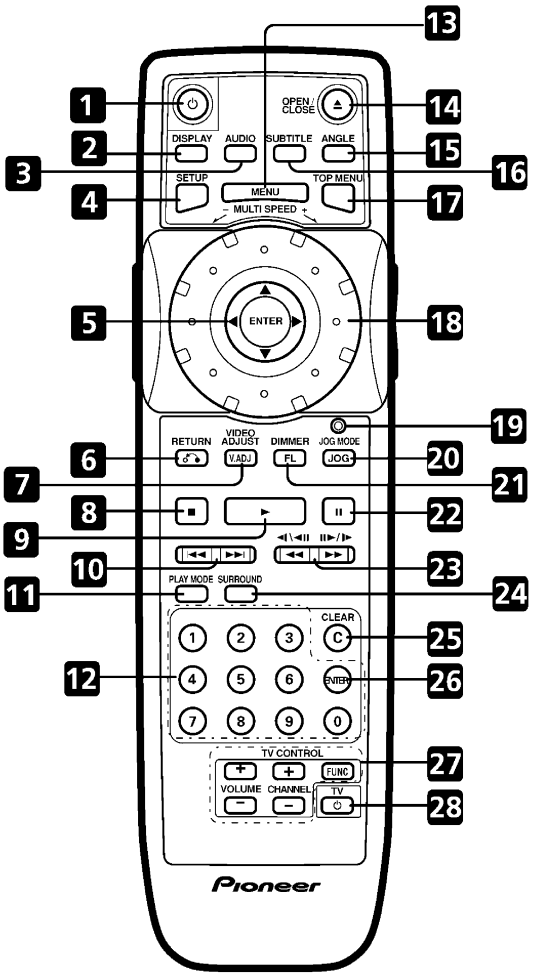
15 D
Lights when a Dolby Digital soundtrack is playing

16 DTS
Lights when a DTS soundtrack is playing

Remote control

Tip

- **DV-47Ai:** All buttons glow slightly in the dark for ease of use.



1 ⏻ (STANDBY/ON)
Press to switch the player on or into standby

2 DISPLAY
Press to display information about the disc playing

3 AUDIO
Press to select the audio channel or language

4 SETUP
Press to display (or exit) the on-screen display

5 ENTER & Joystick
Use to navigate on-screen displays and menus. Press **ENTER** to select an option or execute a command

6 ↶ (RETURN)
Press to return to a previous menu screen

7 V.ADJ (VIDEO ADJUST)
Press to display the Video Adjust menu

8 ■
Press to stop the disc (you can resume playback by pressing ► (play))

9 ►
Press to start or resume playback

10 |◄◄ ►►|
Press to jump to the start of the previous / next chapter / track

11 PLAY MODE
Press to display the Play Mode menu
(You can also get to the Play Mode menu by pressing **SETUP** and selecting **Play Mode**)

12 Number buttons

13 MENU
Press to display a DVD disc menu, or the Disc Navigator if a DVD-RW, CD, Video CD or MP3 disc is loaded

14 ⏏ OPEN/CLOSE
Press to open or close the disc tray

15 ANGLE
Press to change the camera angle during DVD multi-angle scene playback

16 SUBTITLE
Press to select a subtitle display

17 TOP MENU
Press to display the top menu of a DVD disc

18 MULTI DIAL
Use for scanning and slow motion control

19 Jog indicator
Lights when multi dial is in jog mode

20 JOG (JOG MODE)
Press to put switch jog mode on/off. When on, use the **MULTI DIAL** to advance or reverse frames

21 FL (DIMMER)
Press to change the display brightness

22 ⏸
Press to pause playback; press again to restart

23 ◄◄ and ◄❙/◄❙❙ / ►► and ❙❙►/❙►
Use for reverse / forward slow motion playback, frame reverse / advance and reverse / forward scanning.

24 SURROUND
Press to activate/switch off DD V/TruSurround

25 CLEAR
Press to clear a numeric entry

26 ENTER
Press to select an option or execute a command

27 TV CONTROL buttons
VOLUME
Use to adjust the volume

CHANNEL
Use to select TV channel

FUNC
Press FUNC to select the TV for remote control operation

28 ⏻ TV
Press ⏻ TV to turn the TV s power on or put in to standby